

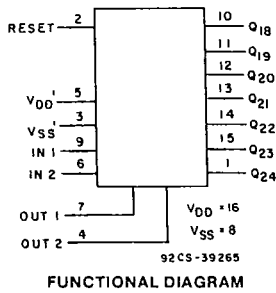
T-45-23-17



# CD4521B Types

## CMOS 24-Stage Frequency Divider

High-Voltage Types (20-Volt Rating)

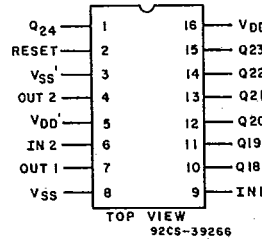


**Features:**

- Reset disables the RC oscillator for low-power standby condition
- V<sub>DD</sub>' and V<sub>SS</sub>' pins are brought out from the crystal oscillator to allow use of external resistors for low-power operation
- Maximum input current of 1 μA at 18 V over full package-temperature range: 100 nA at 18 V and 25°C
- Common reset
- 100% tested for 20-V quiescent current
- 5, 10 and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

■ CD4521B consists of an oscillator section and 24 ripple-carry binary counter stages. The oscillator configuration (using IN1) allows design of either RC or crystal oscillator circuits. IN1 should be tied either HIGH or LOW when not in use. A HIGH on the RESET causes the counter to go to the all-0's state and disables the oscillator. The count is advanced on the negative transition of IN1 (and IN2). A time-saving test mode is described in the Functional Test Sequence Table and in Fig. 6.

The CD4521B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).



**TERMINAL ASSIGNMENT**

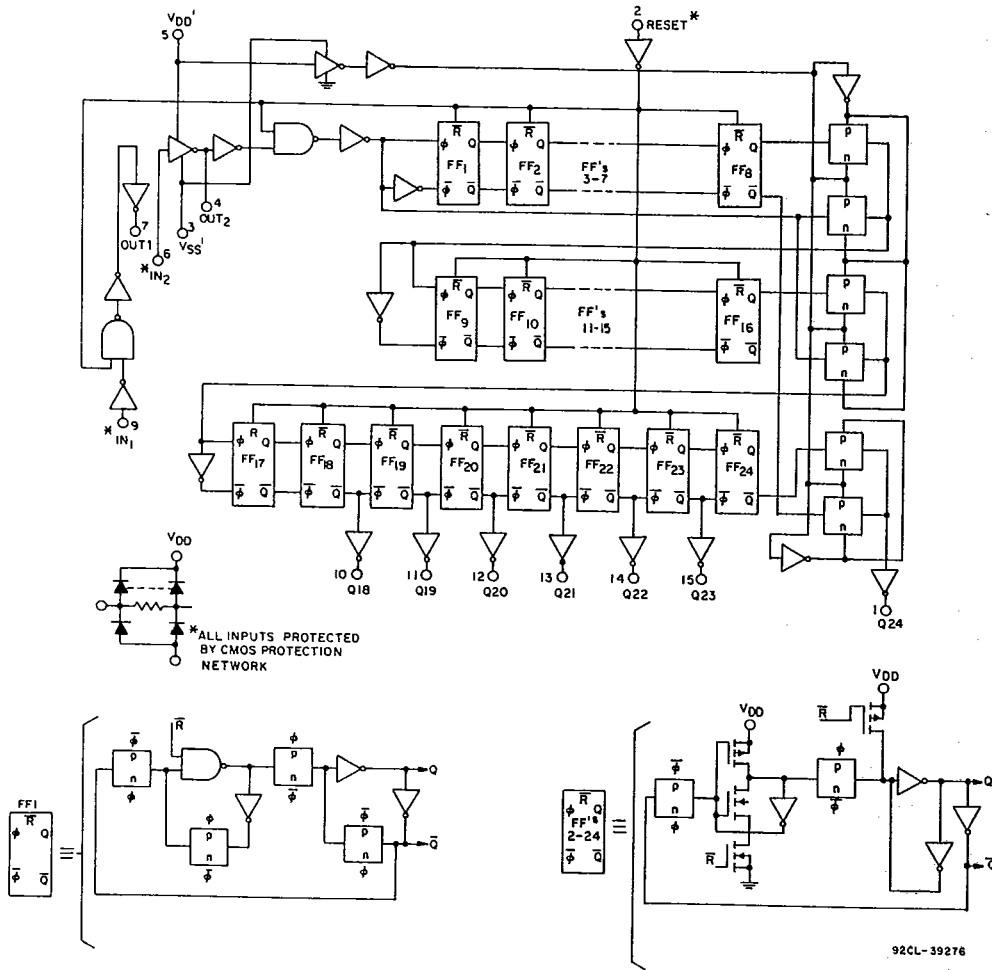
OUTPUT	COUNT CAPACITY
Q18	2 <sup>18</sup> = 262,144
Q19	2 <sup>19</sup> = 524,288
Q20	2 <sup>20</sup> = 1,048,576
Q21	2 <sup>21</sup> = 2,097,152
Q22	2 <sup>22</sup> = 4,194,304
Q23	2 <sup>23</sup> = 8,388,608
Q24	2 <sup>24</sup> = 16,777,216

**MAXIMUM RATINGS, Absolute-Maximum Values:**

- DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)  
Voltages referenced to V<sub>SS</sub> Terminal ..... -0.5V to +20V
- INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V<sub>DD</sub> +0.5V
- DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
- POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):  
For T<sub>A</sub> = -55°C to +100°C ..... 500mW  
For T<sub>A</sub> = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR  
FOR T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW
- OPERATING-TEMPERATURE RANGE (T<sub>A</sub>) ..... -55°C to +125°C
- STORAGE TEMPERATURE RANGE (T<sub>stg</sub>) ..... -65°C to +150°C
- LEAD TEMPERATURE (DURING SOLDERING):  
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

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Fig. 1 - Logic diagram for CD4521B.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	—	0.5	5	5	5	150	150	—	0.04	5	μA
	—	0.10	10	10	10	300	300	—	0.04	10	
	—	0.15	15	20	20	600	600	—	0.04	20	
	—	0.20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
Output High (Source) Current, I <sub>OH</sub> Min.	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	mA
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
	—	0.5	5	0.05	0.05	0.05	0.05	—	0	0.05	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0.10	10	0.05	0.05	0.05	0.05	—	0	0.05	V
	—	0.15	15	0.05	0.05	0.05	0.05	—	0	0.05	
	—	0.5	5	4.95	4.95	4.95	4.95	5	—	—	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0.10	10	9.95	9.95	9.95	9.95	10	—	—	V
	—	0.15	15	14.95	14.95	14.95	14.95	15	—	—	
	—	0.5	5	1.5	1.5	1.5	1.5	—	—	1.5	
Input Low Voltage, V <sub>IL</sub> Max.	0.5,4.5	—	5	1.5	1.5	1.5	1.5	—	—	1.5	V
	1.9	—	10	3	3	3	3	—	—	3	
	1.5,13.5	—	15	4	4	4	4	—	—	4	
Input High Voltage, V <sub>IH</sub> Min.	0.5,4.5	—	5	3.5	3.5	3.5	3.5	3.5	—	—	V
	1.9	—	10	7	7	7	7	7	—	—	
	1.5,13.5	—	15	11	11	11	11	11	—	—	
Input Current, I <sub>IN</sub> Max.	—	0, 18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-9</sup>	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:

CHARACTERISTIC	V <sub>DD</sub> (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T <sub>A</sub> = Full Package-Temperature Range)	—	3	18	V
Input Pulse Width	5	340	—	ns
	10	150	—	
	15	120	—	
Reset Pulse Width	5	180	—	ns
	10	80	—	
	15	50	—	
Input Pulse Frequency	5	—	2	MHz
	10	—	5	
	15	—	6.5	
Input Pulse Rise or Fall Time	5	—	15	μs
	10	—	15	
	15	—	15	
R <sub>T</sub> Operating Range	5	1K	10M	Ω
	10	1K	10M	
	15	1K	10M	
C <sub>T</sub> Operating Range	5	15p	10M	F
	10	15p	10M	
	15	15p	10M	

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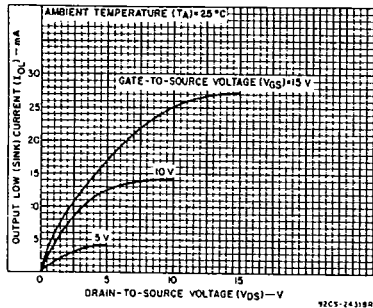


Fig. 2 - Typical output low (sink) current characteristics.

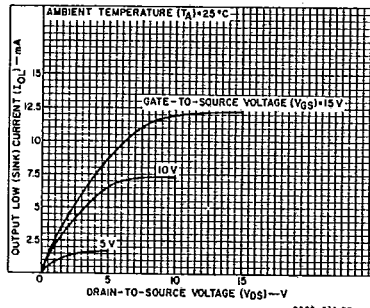


Fig. 3 - Minimum output low (sink) current characteristics.

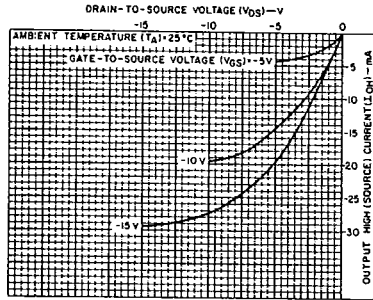


Fig. 4 - Typical output high (source) current characteristics.

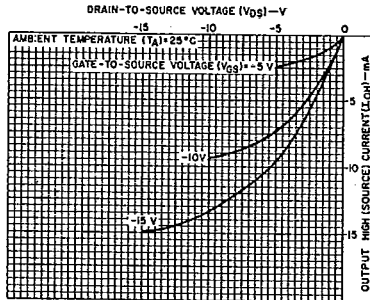


Fig. 5 - Minimum output high (source) current characteristics.

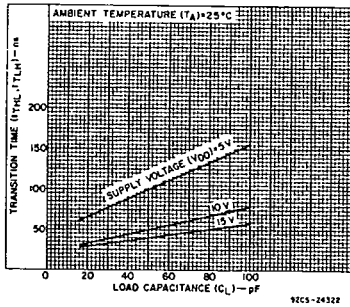


Fig. 6 - Typical transition time as a function of load capacitance.

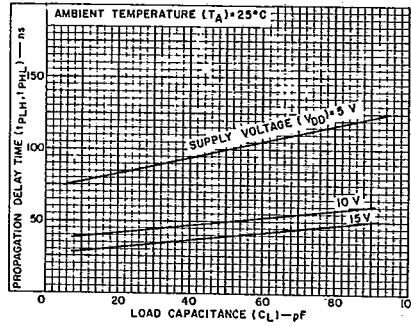


Fig. 7 - Typical propagation delay time ( $Q_n$  to  $Q_n + 1$ ) as a function of load capacitance.

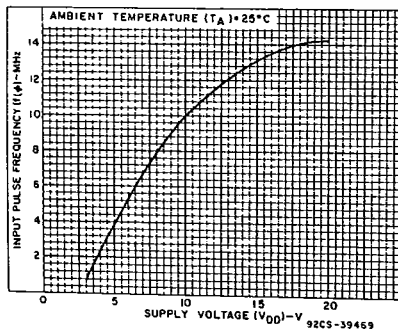


Fig. 8 - Typical maximum input pulse frequency vs. supply voltage.

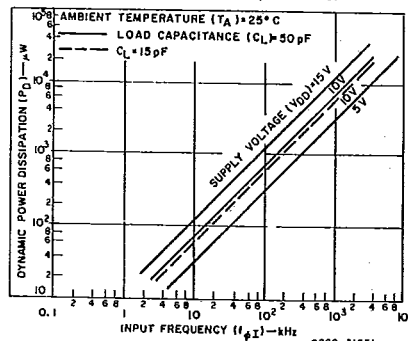


Fig. 9 - Typical dynamic power dissipation as a function of input frequency.

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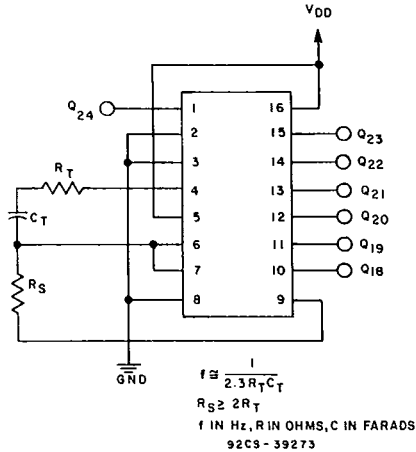


Fig. 10 - RC oscillator circuit.

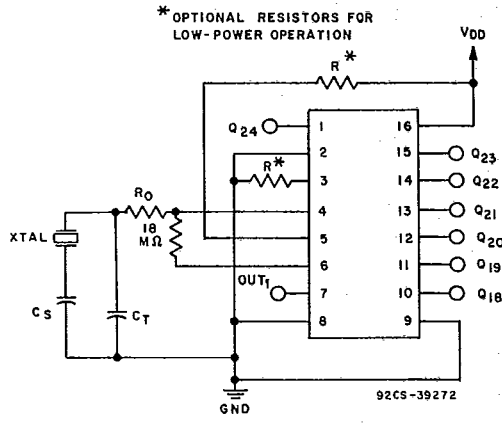


Fig. 11 - Crystal oscillator circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS, At T<sub>A</sub> = 25° C; Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200 Ω

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS		
		V <sub>DD</sub> (V)	Min.	Typ.		Max.	
Propagation Delay Time: Input to Q18	t <sub>PLH</sub> , t <sub>PHL</sub>	5	—	4.5	9	μs	
		10	—	1.7	3.5		
		15	—	1.3	2.7		
Input to Q24		5	—	6	12	μs	
		10	—	2.2	4.5		
		15	—	1.7	3.5		
Reset to Qn		5	—	400	800	ns	
		10	—	170	340		
		15	—	120	240		
Transition Time*	t <sub>THL</sub> , t <sub>LH</sub>	5	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
Minimum Input Pulse Width	t <sub>wφ</sub>	5	—	170	340	ns	
Minimum Reset Pulse Width	t <sub>wRS</sub>	10	—	75	150		
		15	—	60	120		
Maximum Input Pulse Frequency	fφ	5	2	4	—	MHz	
		10	5	10	—		
		15	6.5	13	—		
Input Pulse Rise or Fall Time	t <sub>rφ</sub> , t <sub>fφ</sub>	5	—	—	15	μs	
		10	—	—	15		
		15	—	—	15		
Input Capacitance	C <sub>IN</sub>	Any Input			5	7.5	pF
R <sub>T</sub> Operating Range		5	1K	—	10M	Ω	
		10	1K	—	10M		
		15	1K	—	10M		
C <sub>T</sub> Operating Range		5	15p	—	10μ	F	
		10	15p	—	10μ		
		15	15p	—	10μ		
Maximum Oscillator Frequency	R <sub>T</sub> =1 KΩ C <sub>T</sub> =15 pF R <sub>S</sub> =30 KΩ	5	0.5	0.7	0.9	MHz	
		10	1.2	1.5	1.8		
		15	1.7	2.1	2.5		

\*Not applicable for pin 4 (OUT2).

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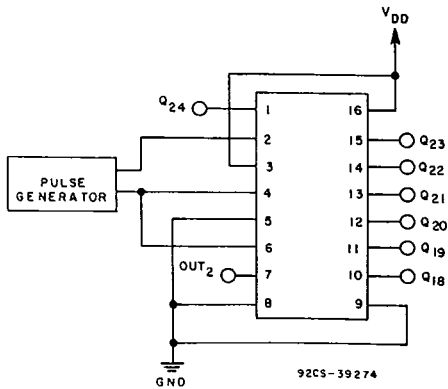


Fig. 12 - Functional test circuit.

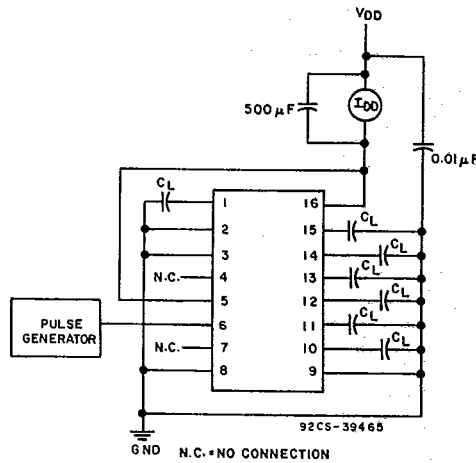


Fig. 13 - Dynamic power dissipation test circuit.

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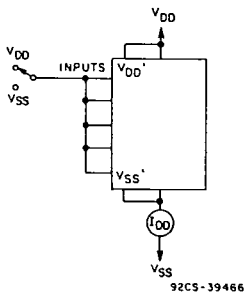


Fig. 14 - Quiescent device current.

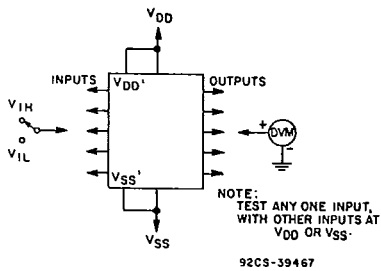


Fig. 15 - Input voltage.

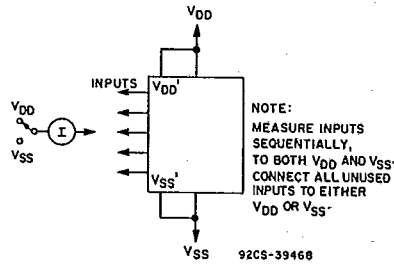


Fig. 16 - Input current.

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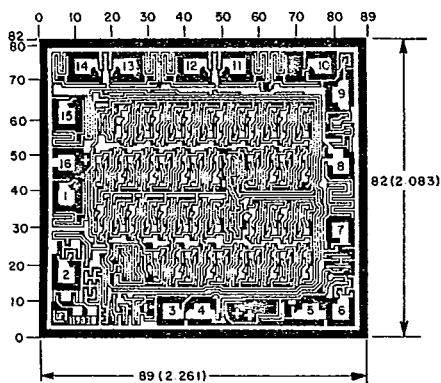
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FUNCTIONAL TEST SEQUENCE

INPUTS		OUTPUTS				COMMENTS
RESET	IN 2	OUT 2	V <sub>SS</sub> '	V <sub>DD</sub> '	Q18-Q24	
1	0	0	V <sub>DD</sub>	V <sub>SS</sub>	LOW	Counter is in three 8-stage sections in parallel mode. Counter is reset. IN 2 and OUT 2 are tied together.
0	1	1	V <sub>DD</sub>	V <sub>SS</sub>		First LOW-to-HIGH transition at IN 2.
0	0	0	V <sub>DD</sub>	V <sub>SS</sub>		255 LOW-to-HIGH transitions are clocked in at IN 2.
	1	1				
	—	—				
	—	—				
0	1	1	V <sub>DD</sub>	V <sub>SS</sub>	HIGH	The 255th LOW-to-HIGH transition.
0	0	0	V <sub>DD</sub>	V <sub>SS</sub>	HIGH	Counter is converted back to 24-stage serial-mode operation.
0	0	0	V <sub>SS</sub>	V <sub>SS</sub>	HIGH	
0	1	0	V <sub>SS</sub>	V <sub>DD</sub>	HIGH	
0	1		V <sub>SS</sub>	V <sub>DD</sub>	HIGH	
0	0		V <sub>SS</sub>	V <sub>DD</sub>	LOW	OUT 2 reverts to output operation.
0	0		V <sub>SS</sub>	V <sub>DD</sub>	LOW	Counter ripples from an all-HIGH state to an all-LOW state.

A test function, which divides, has been included to reduce the time required to test all 24 stages of the counter. Three sections are loaded in parallel to 255 counts, forcing all the outputs to be in the HIGH state. The counter is changed

back to serial-mode operation and one additional LOW-to-HIGH transition is entered at IN 2, which causes the outputs to ripple from an all-HIGH state to an all-LOW state.



92CS-39275  
Dimensions and pad layout for CD4521BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10<sup>-3</sup> inch).