74195, LS195A, S195
Shift Registers

4-Bit Parallel Access Shift Register
Product Specification

Logic Products

FEATURES
- **Buffered Clock and Control inputs**
- **Shift right and parallel load capability**
- **J-$\overline{K}$ (D) inputs to first stage**
- **Complement output from last stage**
- **Asynchronous Master Reset**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74195	39MHz	39mA
74LS195A	39MHz	14mA
74S195	105MHz	70mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74195N, N74LS195N, N74S195N
Plastic SO-16	N74LS195AD

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
All	Inputs	1ul	1Sul	1LSul
All	Outputs	10ul	10Sul	10LSul

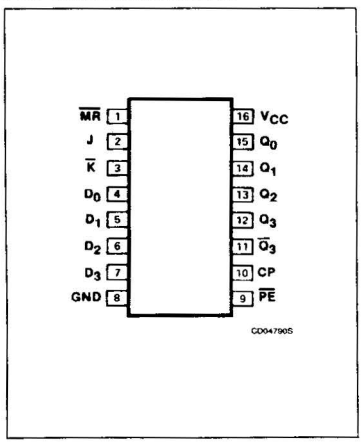
NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION
The functional characteristics of the '195 4-Bit Parallel Access Shift register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

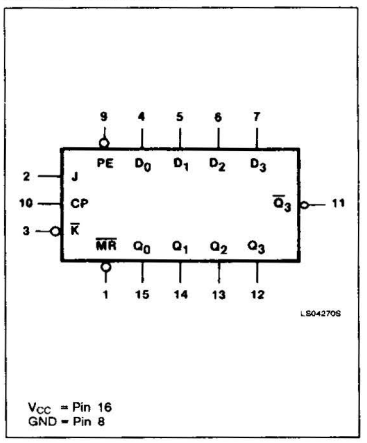
The '195 operates on two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH, and is shifted 1 bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition.

The J and $\overline{K}$ inputs provide the flexibility of the JK type input for special applications and, by tying the two pins together, the simple D type input for general applications. The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs ($D_0 - D_3$) is transferred to the respective $Q_0 - Q_3$ outputs.

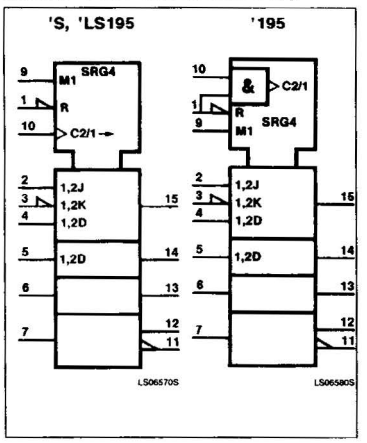
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

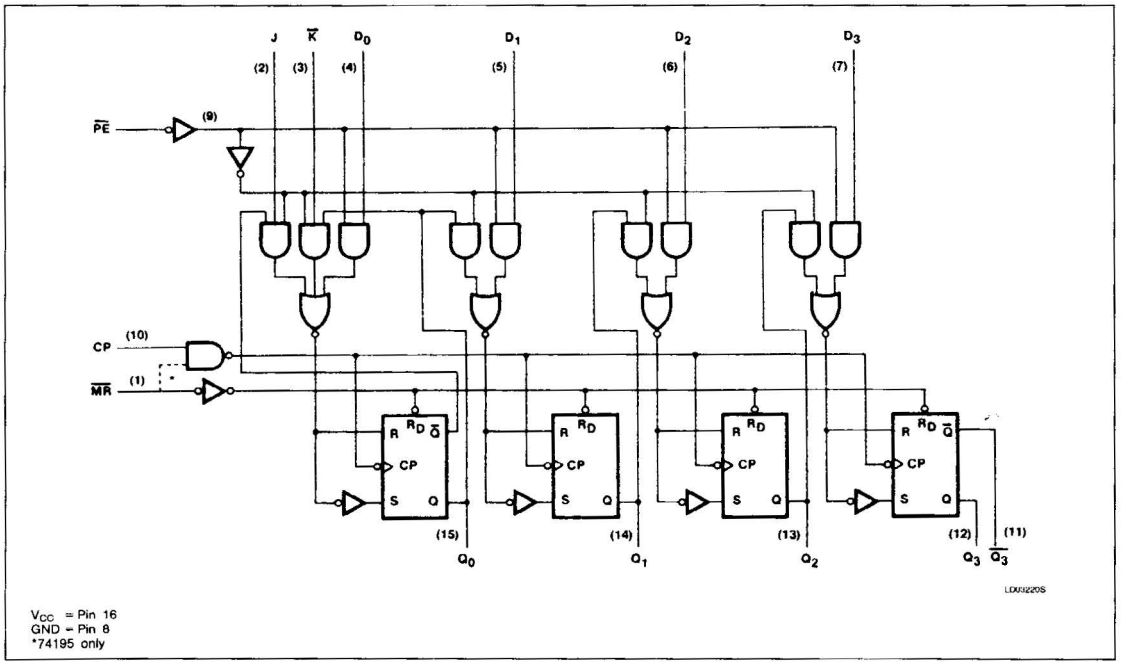


Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1}) inputs and holding the $\overline{PE}$ input low.

All parallel and serial data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. The '195 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the set-up and release time requirements.

A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition. The $\overline{MR}$ on the 54/74195 is gated with the clock. Therefore, the LOW-to-HIGH $\overline{MR}$ transition should only occur while the clock is LOW to avoid false clocking on the 54/74195.

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous reset	L	X	X	X	X	X	L	L	L	L	H
Shift, set first stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, reset first stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, toggle first stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, retain first stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

H = HIGH voltage level.
L = LOW voltage level.
X = Don't care.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current			−12			−18			−18	mA
I_{OH}	HIGH-level output current			−800			−400			−1000	μA
I_{OL}	LOW-level output current			16			8			20	mA
T_A	Operating free-air temperature	0		70	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74195			74LS195A			74S195			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{IL} = MAX, I_{OH} = MAX		2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA (74LS)					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5			−1.5			−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V			1.0						1.0	mA
			V_I = 7.0V						0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V			40							μA
			V_I = 2.7V						20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V			−1.6			−0.4				mA
			V_I = 0.5V									−2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−18		−57	−20		−100	−40		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			39	63		14	21		70	109	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open, $\overline{PE}$ grounded, and 4.5V applied to the J, $\overline{K}$, and Data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V to $\overline{MR}$, and then a momentary ground, followed by 4.5V to clock.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

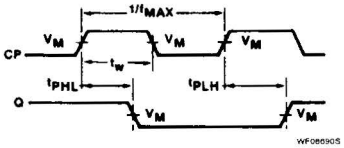
PARAMETER		TEST CONDITIONS	74		74LS		74S		UNIT
			$C_L = 15pF$, $R_L = 400\Omega$		$C_L = 15pF$, $R_L = 2k\Omega$		$C_L = 15pF$, $R_L = 280\Omega$		
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		30		70		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		22 26		22 26		12 16.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		30		30		18.5	ns

NOTE:
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

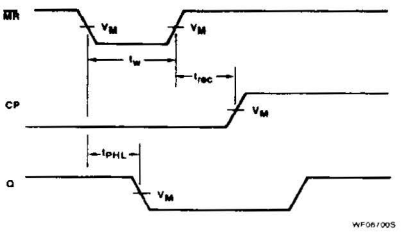
PARAMETER		TEST CONDITIONS	74		74LS		74S		UNIT
			Min	Max	Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	16		16		7		ns
t_W	Master Reset pulse width	Waveform 2	12		12		12		ns
t_s	Set-up time, J, $\overline{K}$ and data to clock	Waveform 3	20		15		5.0		ns
t_h	Hold time, J, $\overline{K}$ and data to clock	Waveform 3	0		0		3.0		ns
t_s	Set-up time, $\overline{PE}$ to clock	Waveform 4	25		25		11		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 4	0		0		0		ns
t_{rec}	Recovery time, $\overline{MR}$ to clock	Waveform 2	25		25		9.0		ns

AC WAVEFORMS



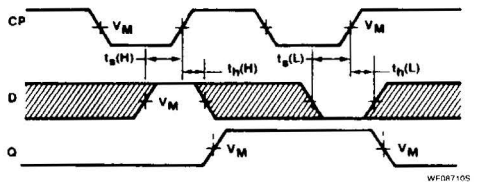
$V_M = 1.5V$ for 74 and 74S, $V_M = 1.5V$ for 74LS.

Waveform 1. Clock To Output Delays And Clock Pulse Width



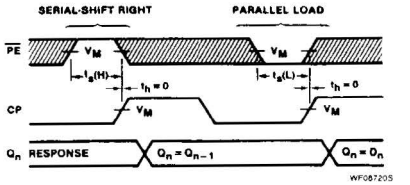
$V_M = 1.5V$ for 74 and 74S; $V_M = 1.5V$ for 74LS.

Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



$V_M = 1.5V$ for 74 and 74S; $V_M = 1.5V$ for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

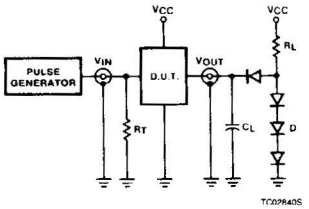
Waveform 3. Data Set-up And Hold Times

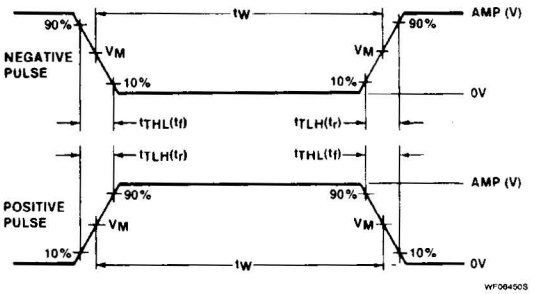


$V_M = 1.5V$ for 74 and 74S; $V_M = 1.5V$ for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 4. Set-up And Hold Times Parallel Enable To Clock

TEST CIRCUITS AND WAVEFORMS





V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

5