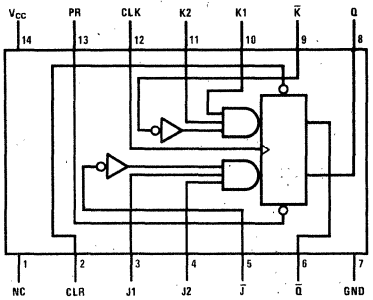
70 AND-Gated J-K Positive-Edge-Triggered Flip-Flops with Preset and Clear

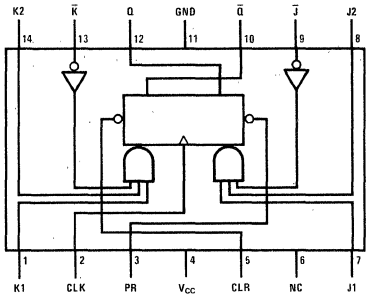


5470/7470(J),(N)

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	L	X	X	H	L
H	L	L	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	Q0	$\overline{Q}$0
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	H	H	TOGGLE	
H	H	L	X	X	Q0	$\overline{Q}$0

$J = J1 \cdot J2 \cdot \overline{J}$
$K = K1 \cdot K2 \cdot \overline{K}$
If inputs $\overline{J}$ and $\overline{K}$ are not used, they must be grounded.
Preset or Clear function can occur only when clock input is low.



5470/7470(W)

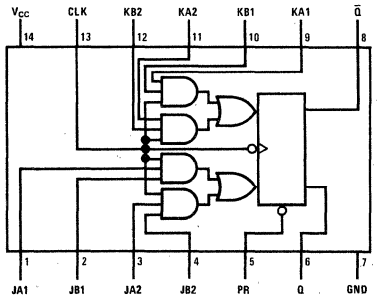
See page 1-62 for electrical tables.

H71 AND-OR-Gated J-K Master-Slave Flip-Flops with Preset

TRUTH TABLE

INPUTS				OUTPUTS	
PR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	⎍	L	L	Q0	$\overline{Q}$0
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

$J = (J1A \cdot J1B) + (J2A \cdot J2B)$
$K = (K1A \cdot K1B) + (K2A \cdot K2B)$

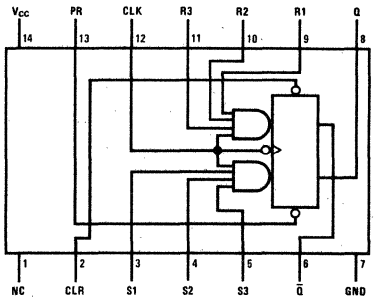


54H71/74H71(J),(N)

See page 1-64 for electrical tables.

Notes: ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

L71 AND-Gated R-S Master-Slave Flip-Flops with Preset and Clear

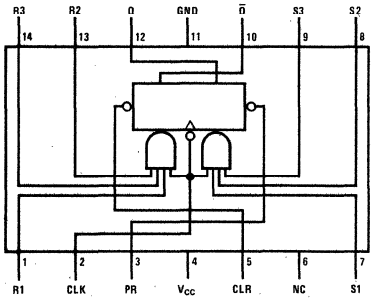


54L71/74L71(J),(N)

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	S	R	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q0	$\bar{Q}$0
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	INDETER-MINATE	

R = R1 · R2 · R3
S = S1 · S2 · S3



54L71/74L71(W)

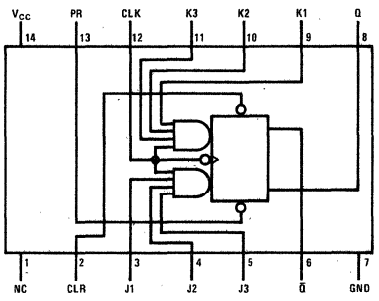
See page 1-66 for electrical tables.

72 AND-Gated J-K Master-Slave Flip-Flops with Preset and Clear

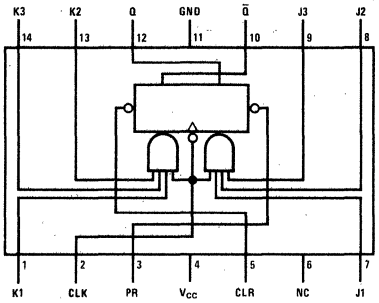
TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q0	$\bar{Q}$0
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

J = J1·J2·J3
K = K1·K2·K3



5472/7472(J),(N);54H72/74H72(J),(N);
54L72/74L72(J),(N)



5472/7472(W);54L72/74L72(W)

See page 1-62 (72), 1-64 (H72), 1-66 (L72) for electrical tables.

Notes: ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

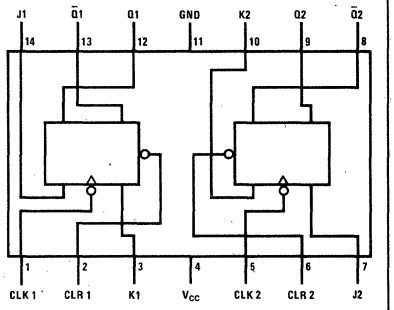
73 Dual J-K Flip-Flops with Clear

TRUTH TABLE
73, H73, L73

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q0	$\bar{Q}$0
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

TRUTH TABLE
LS73

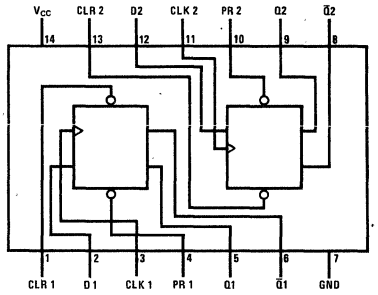
INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\bar{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\bar{Q}$0



5473/7473(J), (N), (W); 54H73/74H73(J), (N); 54L73/74L73 (J), (N), (W); 54LS73/74LS73(J), (N), (W)

See page 1-62 (73), 1-64 (H73), 1-66 (L73), 1-68 (LS73) for electrical tables.

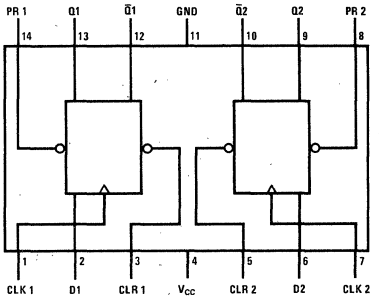
74 Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear



5474/7474(J),(N); 54H74/74H74(J),(N); 54L74/74L74(J),(N); 54LS74/74LS74(J),(N),(W); 74S74(N)

TRUTH TABLE

INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\bar{Q}$0



5474/7474(W); 54L74/74L74(W)

See page 1-62 (74), 1-64 (H74), 1-66 (L74), 1-68 (LS74), 1-70 (S74) for electrical tables.

Notes: ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

Q0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

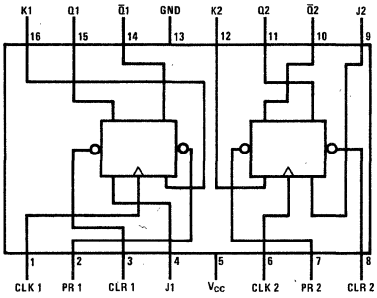
76 Dual J-K Flip-Flops with Preset and Clear

TRUTH TABLE
76, H76

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q0	$\bar{Q}$0
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

TRUTH TABLE
LS76

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\bar{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\bar{Q}$0



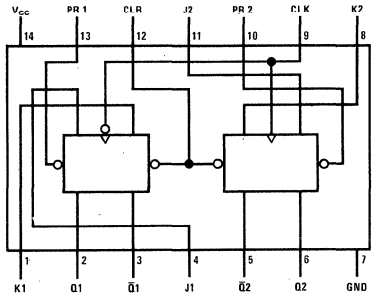
5476/7476(J), (N), (W); 54H76/74H76(J), (N); 54LS76/74LS76(J), (N), (W)

See page 1-62 (76), 1-64 (H76), 1-68 (LS76) for electrical tables.

78 Dual J-K Flip-Flops with Preset, Common Clear, and Common Clock

TRUTH TABLE
H78, L78

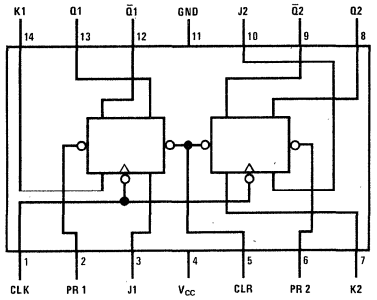
INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q0	$\bar{Q}$0
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	



54H78/74H78(J),(N)

TRUTH TABLE
LS78

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\bar{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\bar{Q}$0



54L78/74L78(J), (N), (W); 54LS78/74LS78(J), (N), (W)

See page 1-64 (H78), 1-66 (L78), 1-68 (LS78) for electrical tables.

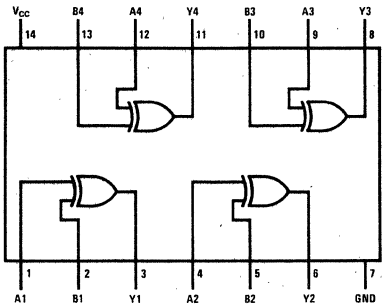
Notes: ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

Q0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

86 Quad 2-Input EXCLUSIVE-OR Gates

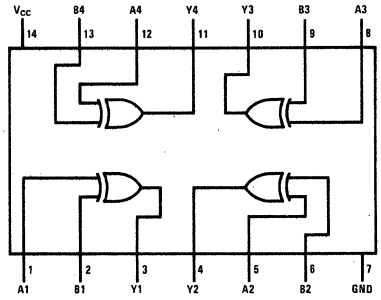


5486/7486(J), (N), (W);
54LS86/74LS86(J), (N), (W); 74S86(N)

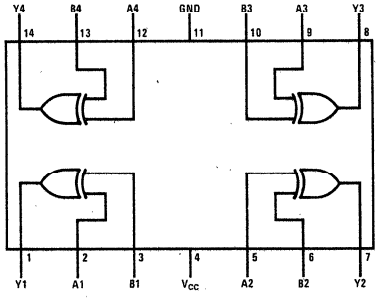
TRUTH TABLE
(86, L86, LS86, S86)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

$Y = A \oplus B = \overline{A}B + A\overline{B}$



54L86/74L86(J),(N)



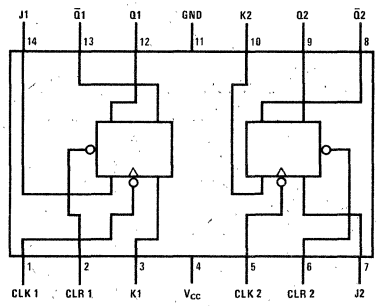
54L86/74L86(W)

See page 1-72 for electrical tables.

103 Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

TRUTH TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0



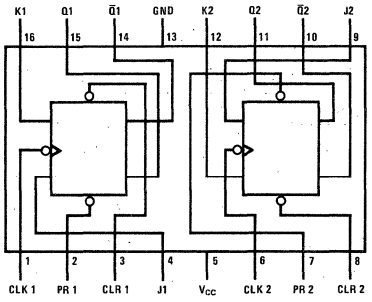
54H103/74H103(J),(N)

See page 1-74 for electrical tables.

106 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0



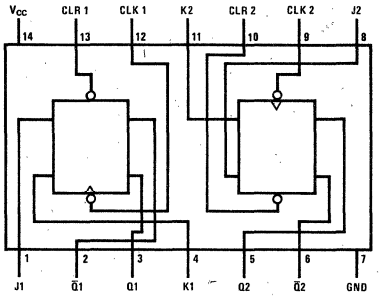
54H106/74H106(J), (N)

See page 1-74 for electrical tables.

107 Dual J-K Master-Slave Flip-Flops with Clear

TRUTH TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⊓	L	L	Q0	$\overline{Q}$0
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	TOGGLE	



54107/74107(J),(N);
54LS107/74LS107(J), (N), (W)

See page 1-62 (107), 1-68 (LS107) for electrical tables.

Notes: ⊓ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

Q0 = the level of Q before the indicated input conditions were established.

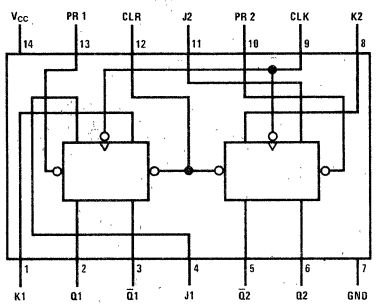
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

108 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset, Common Clear, and Common Clock

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0



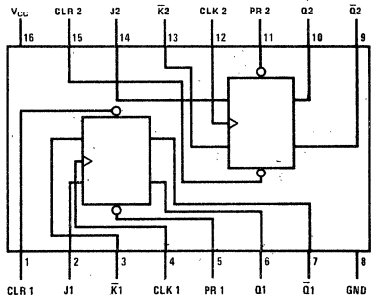
54H108/74H108(J), (N)

See page 1-74 for electrical tables.

109 Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flops with Preset and Clear

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\overline{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0



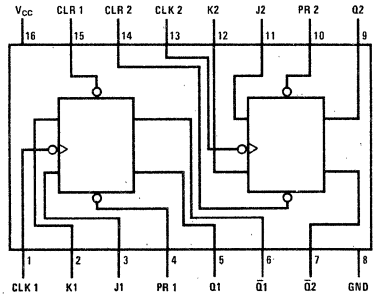
54109/74109(J), (N), (W);
54LS109/74LS109(J), (N), (W)

See page 1-62 (109), 1-68 (LS109) for electrical tables.

112 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0



54LS112/74LS112(J), (N), (W); 74S112(N)

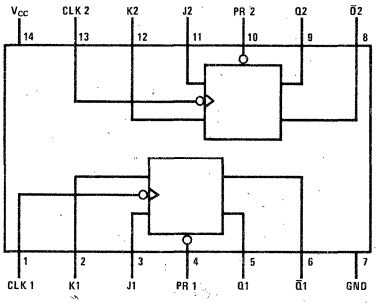
See page 1-68 (LS112), 1-70 (S112) for electrical tables.

Notes: Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

113 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset

TRUTH TABLE

INPUTS				OUTPUTS	
PR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q0	$\bar{Q}0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\bar{Q}0$



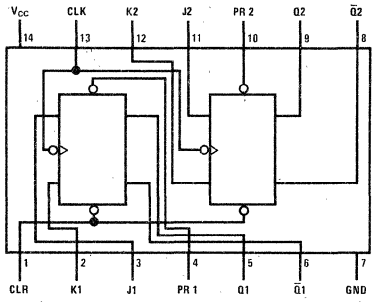
54LS113/74LS113(J), (N), (W); 74S113(N)

See page 1-68 (LS113), 1-70 (S113) for electrical tables.

114 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset, Common Clear, and Common Clock

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\bar{Q}0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\bar{Q}0$



54LS114/74LS114(J), (N), (W); 74S114(N)

See page 1-68 (LS114), 1-70 (S114) for electrical tables.

Notes: Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			CONDITIONS		DM54/74												UNITS
					70			72, 73, 76, 107			74			109			
					MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage				2			2			2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8			0.8			0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−1.5			−1.5			−1.5			−1.5	V
I_{OH}	High Level Output Current						−400			−400			−400			−1200	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = Max		2.4	3.4		2.4	3.4		2.4	3.4		2.4			V
I_{OL}	Low Level Output Current						16			16			16			16	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA			0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V				1			1			1			1	mA
I_{IH}	High Level Input Current	D, J, K, or $\overline{K}$	V_{CC} = Max, V_I = 2.4V				40			40			40			40	μA
		Clear					80			80			120			160	
		Preset					80			80			40			80	
		Clock					40			80			80			80	
I_{IL}	Low Level Input Current	D, J, K, or $\overline{K}$	V_{CC} = Max, V_I = 0.4V				−1.6			−1.6			−1.6			−1.6	mA
		Clear					−3.2			−3.2			−3.2			−4.8	
		Preset					−3.2			−3.2			−1.6			−3.2	
		Clock					−1.6			−3.2			−3.2			−3.2	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)	DM54	−20		−57	−20		−55	−20		−55	−30	−55	−85	mA
				DM74	−18		−57	−18		−55	−18		−55	−30	−55	−85	
I_{CC}	Supply Current (Average per Flip-Flop)		V_{CC} = Max(3)			13	26		9	17		8.5	15		10	15	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is at 4.5V for the 70, and is grounded for all the others.

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

PARAMETER			FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54/74											UNITS
						70			72, 73, 76, 107			74			109			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum Clock Frequency				C_L = 15 pF, R_L = 400Ω	20	35		15	20		20	25		30	40		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Preset (as applicable)	Q				50		16	25			25		9	14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			$\overline{Q}$				50		25	40			40		18	29	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clear (as applicable)	$\overline{Q}$				50		16	25			25		9	14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			Q				50		25	40			40		17	25	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Q or $\overline{Q}$			27	50		16	25		14	25		12	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						18	50		25	40		20	40		19	28	
t_W	Pulse Width	Clock High				20			20			30			20			ns
		Clock Low				30			47			37			20			
		Preset or Clear Low				25			25			30			20			
t_{SETUP}	Input Setup Time(4)					20↑			0↑			20↑			15↑			ns
t_{HOLD}	Input Hold Time(4)					5↑			0↓			5↑			10↑			ns

Notes

(4) ↑ ↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.