TTL/MSI 9390/5490, 7490
DECADE COUNTER

DESCRIPTION – The TTL/MSI 9390/5490, 7490 is a Decade Counter which consists of four dual rank, master slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Count inputs are inhibited, and all outputs are returned to logical zero or a binary coded decimal (BCD) count of 9 through gated direct reset lines. The output from flip-flop A is not internally connected to the succeeding stages, therefore the count may be separated into these independent count modes:

A. If used as a binary coded decimal decade counter, the $\overline{CP}_{BD}$ input must be externally connected to the Q_A output. The $\overline{CP}_A$ input receives the incoming count, and a count sequence is obtained in accordance with the BCD count for nine's complement decimal application.

B. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the Q_D output must be externally connected to the $\overline{CP}_A$ input. The input count is then applied at the $\overline{CP}_{BD}$ input and a divide-by-ten square wave is obtained at output Q_A.

C. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The $\overline{CP}_{BD}$ input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

PIN NAMES		LOADING
R_0	Reset-Zero Inputs	1 U.L.
R_9	Reset-Nine Inputs	1 U.L.
$\overline{CP}_A$	Clock Input	2 U.L.
$\overline{CP}_{BD}$	Clock Input	4 U.L.
Q_A, Q_B, Q_C, Q_D	Outputs	10 U.L.

1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.

BCD COUNT SEQUENCE (Note 1)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

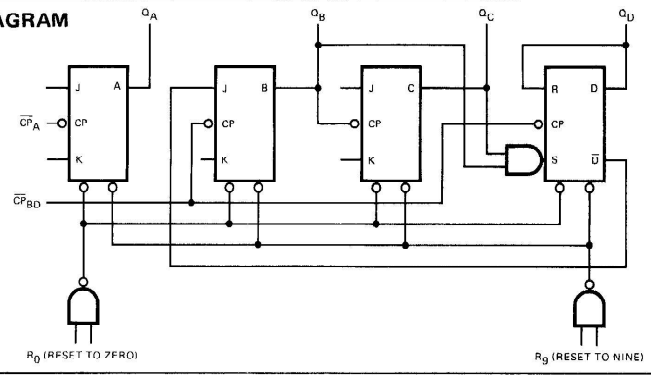
TRUTH TABLES

RESET/COUNT (see Note 2)

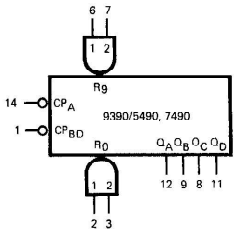
RESET INPUTS				OUTPUT
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	$Q_D Q_C Q_B Q_A$
H	H	L	X	L L L L
H	H	X	L	L L L L
X	X	H	H	H L L H
X	L	X	L	COUNT
L	X	L	X	COUNT
L	X	X	L	COUNT
X	L	L	X	COUNT

NOTES:
1. Output Q_A connected to input CP_{BD} for BCD count.
2. X indicates that either a HIGH level or a LOW level may be present.

LOGIC DIAGRAM

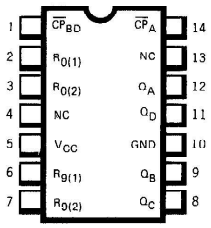


LOGIC SYMBOL

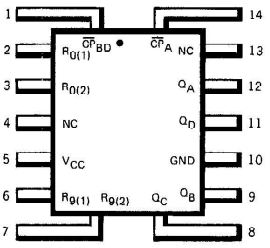


V_{CC} = Pin 5
GND = Pin 10
NC = Pin 4, 13

CONNECTION DIAGRAM DIP (TOP VIEW)



FLAT PAK (TOP VIEW)



Positive logic: See Truth Table.
NC – No internal connection.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9390XM/5490XM			9390XC/7490XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	-55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N (Note 5)			10			10	U.L.
Width of Input Count Pulse, $t_{p(in)}$	50			50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			50			ns

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = -0.4 mA		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		1
I_{IH}	Input HIGH Current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Input $\overline{CP}_A$			80	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Input $\overline{CP}_{BD}$			160	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
	Input LOW Current at Input $\overline{CP}_A$			-3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
	Input LOW Current at Input $\overline{CP}_{BD}$			-6.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
I_{OS}	Output Short Circuit Current (Note 3)	-20		-57	mA	9390/5490	V_{CC} = MAX.	5
		-18		-57	mA	9390/7490		
I_{CC}	Supply Current		32	46	mA	9390/5490	V_{CC} = MAX.	3
			32	53	mA	9390/7490		

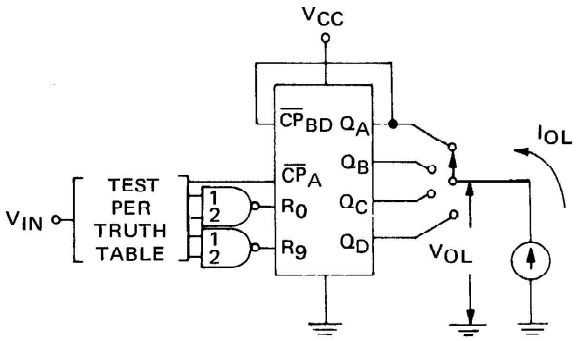
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Frequency of Input Count Pulse	10	18		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	
t_{PLH}	Turn Off Delay from Input Count Pulse to Output Q_C		60	100	ns		A
t_{PHL}	Turn On Delay from Input Count Pulse to Output Q_C		60	100	ns		A

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.
(5) Fan out from output Q_A to input $\overline{CP}_{BD}$ and to 10 additional series 54/74 loads is permitted.

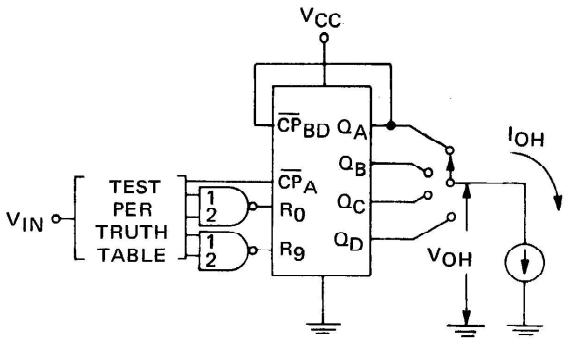
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUIT*



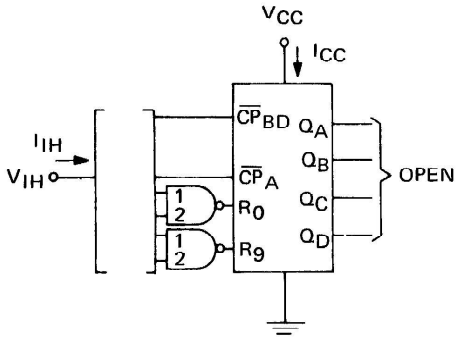
1. Each output is tested in the LOW level state.

Fig. 1



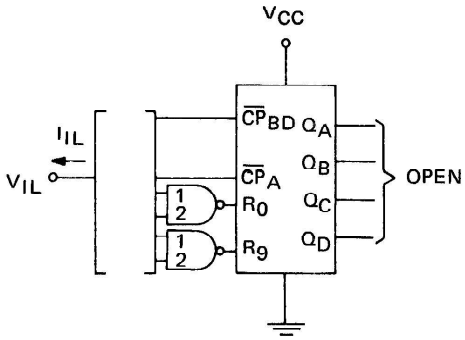
1. Each output is tested in the HIGH level state.

Fig. 2



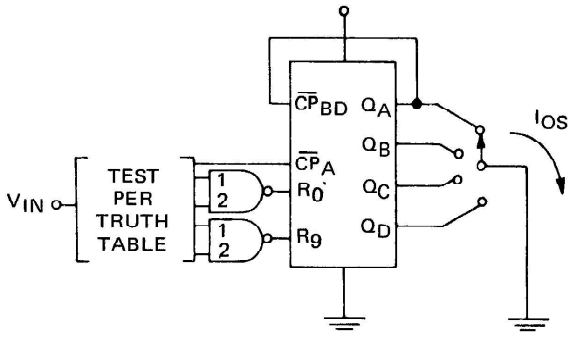
1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ ground $R_{0(2)}$ or $R_{9(2)}$.
3. When testing $R_{0(2)}$ or $R_{9(2)}$ ground $R_{0(1)}$ or $R_{9(1)}$.
4. When testing I_{CC} reset all outputs to LOW level, ground all inputs, then measure I_{CC}.

Fig. 3



1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ apply 4.5 V to $R_{0(2)}$ or $R_{9(2)}$.
3. When testing $R_{0(2)}$ or $R_{9(2)}$ apply 4.5 V to $R_{0(1)}$ or $R_{9(1)}$.

Fig. 4



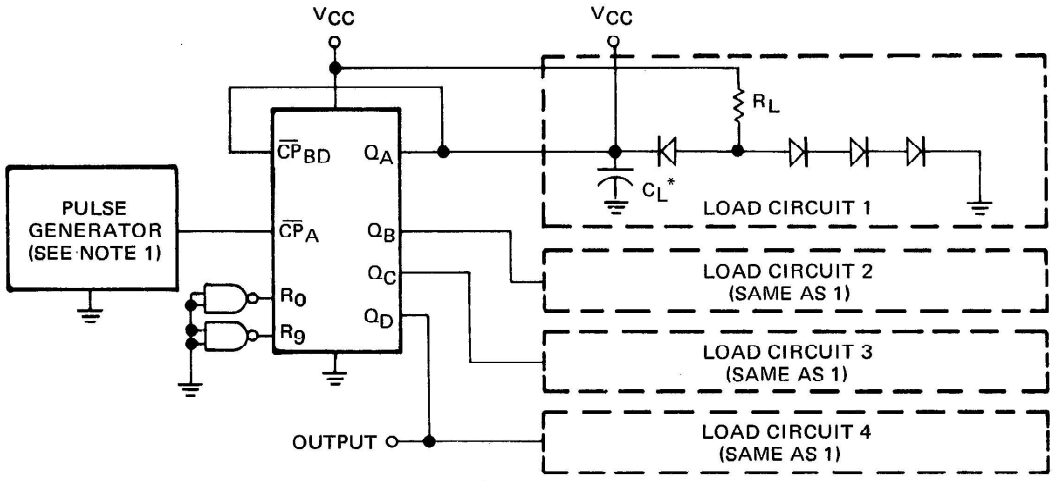
1. Each output is tested in the HIGH level state.

Fig. 5

*Arrows indicate actual direction of current flow.

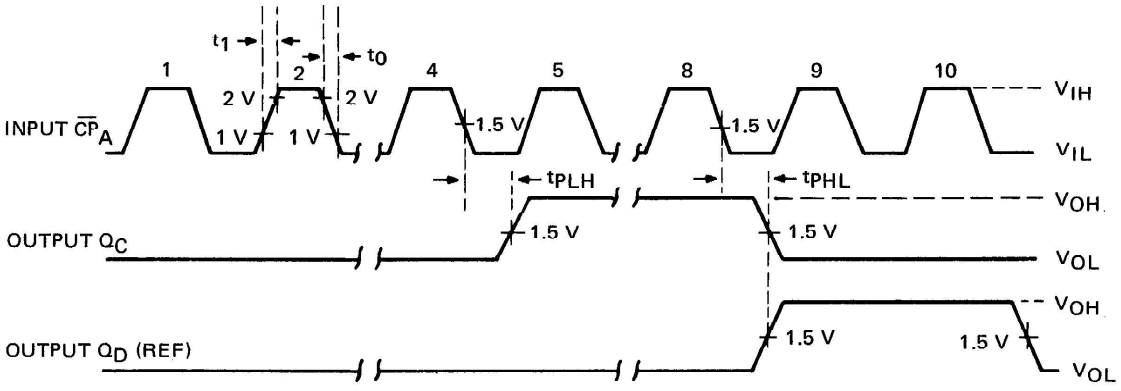
PARAMETER MEASUREMENT INFORMATION (Con't.)

SWITCHING CHARACTERISTICS



*C_L includes probe and jig capacitance.

TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.
2. Propagation Delay = $\frac{t_{PHL} + t_{PLH}}{2}$
3. Voltage values are with respect to ground terminal.

Fig. A – SWITCHING TIMES

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