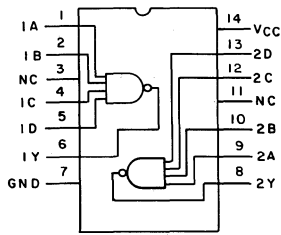


CD54/74HC20 CD54/74HCT20

High-Speed CMOS Logic



92CS-38338
**FUNCTIONAL DIAGRAM AND
TERMINAL ASSIGNMENT**

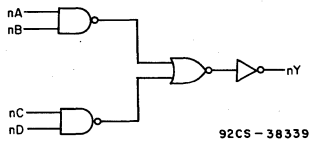
Dual 4-Input NAND Gate

Type Features:

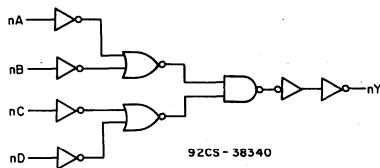
- Buffered inputs (HCT types)
- Typical propagation delay = 8 ns
@ $V_{CC} = 5V$, $C_L = 15 pF$, $T_A = 25^\circ C$ (HC types)

The RCA-CD54/74HC20 and CD54/74HCT20 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC20 and CD54HCT20 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC20 and CD74HCT20 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).



92CS-38339
HC LOGIC DIAGRAM (1 GATE)



92CS-38340
HCT LOGIC DIAGRAM (1 GATE)

Family Features

- Fanout (over temperature range):
Standard outputs — 10 LSTTL loads
Bus driver outputs — 15 LSTTL loads
- Wide operating temperature range:
CD74HC/HCT: -40 to +85° C
- Balanced Propagation Delay and Transition Times
- Significant power reduction compared to LSTTL logic ICs
- Alternate source is Philips/Signetics
- CD54HC/CD74HC types:
2 to 6 V operation
High noise immunity:
 $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} ; @ $V_{CC} = 5V$
- CD54HCT/CD74HCT types:
4.5 to 5.5 V operation
Direct LSTTL input logic compatibility
 $V_{IL} = 0.8 V$ max., $V_{IH} = 2 V$ min.
CMOS input compatibility
 $I_I \leq 1 \mu A$ @ V_{OL} , V_{OH}

TRUTH TABLE

INPUTS				OUTPUTS
nA	nB	nC	nD	nY
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

X = Don't Care

L = Low Voltage Level
H = High Voltage Level

CD54/74HC20 CD54/74HCT20

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V _{cc}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I _{IK} (FOR V _i < -0.5 V OR V _i > V _{cc} +0.5 V)	± 20 mA
DC OUTPUT CURRENT, I _{OK} (FOR V _o < -0.5 V OR V _o > V _{cc} +0.5 V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I _o) (FOR -0.5 V < V _o < V _{cc} +0.5 V)	± 25 mA
DC V _{cc} OR GROUND CURRENT (I _{cc})	± 50 mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T _A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T _A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T _{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package Temperature Range) V _{cc} :* CD54/74HC Types CD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V _i , V _o	0	V _{cc}	V
Operating Temperature T _A : CD74 Types CD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall Times, t _r , t _f at 2V at 4.5 V at 6V	0 0 0	1000 500 400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC20 CD54/74HCT20

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC20/CD54HC20										CD74HCT20/CD54HCT20								UNITS	
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V _i V	I _o mA	V _{cc} V	+25°C			-40/ +85°C		-55/ +125°C		V _i V	V _{cc} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min		Max
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5								V
			4.5	3.15	—	—	3.15	—	3.15	—	—	to 5.5								
			6	4.2	—	—	4.2	—	4.2	—	—									
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5								V
			4.5	—	—	1.35	—	1.35	—	1.35	—	to 5.5								
			6	—	—	1.8	—	1.8	—	1.8	—									
High-Level Output Voltage V _{O_H}	V _{IL}		2	1.9	—	—	1.9	—	1.9	—	V _{IL}									V
or	-0.02		4.5	4.4	—	—	4.4	—	4.4	—	or 4.5	4.4	—	—	4.4	—	4.4	—	—	V
CMOS Loads	V _{IH}		6	5.9	—	—	5.9	—	5.9	—	V _{IH}									
TTL Loads	V _{IL}										V _{IL}									V
or	-4		4.5	3.98	—	—	3.84	—	3.7	—	or 4.5	3.98	—	—	3.84	—	3.7	—	—	V
	V _{IH}		6	5.48	—	—	5.34	—	5.2	—	V _{IH}									
Low-Level Output Voltage V _{O_L}	V _{IL}		2	—	—	0.1	—	0.1	—	0.1	V _{IL}									V
or	0.02		4.5	—	—	0.1	—	0.1	—	0.1	or 4.5	—	—	0.1	—	0.1	—	0.1	—	V
CMOS Loads	V _{IH}		6	—	—	0.1	—	0.1	—	0.1	V _{IH}									
TTL Loads	V _{IL}										V _{IL}									V
or	4		4.5	—	—	0.26	—	0.33	—	0.4	or 4.5	—	—	0.26	—	0.33	—	0.4	—	V
	V _{IH}		5.2	6	—	—	0.26	—	0.33	—	0.4	V _{IH}								
Input Leakage Current I _i	V _{cc}		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{cc} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
or	Gnd																			
Quiescent Device Current I _{cc}	V _{cc}	0	6	—	—	2	—	20	—	40	V _{cc}	5.5	—	—	2	—	20	—	40	μA
or	Gnd										or 5.5									
Additional Quiescent Device Current per input pin: 1 unit load ΔI _{cc} *											V _{cc} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_i = 2.4 V, V_{cc} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All	0.15

*Unit load is ΔI_{cc} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC20 CD54/74HCT20

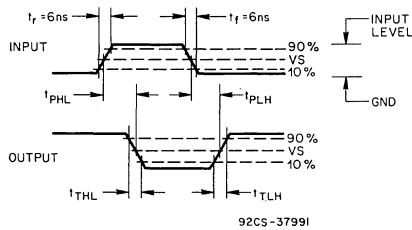
SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input t_r , $t_f = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	TYPICAL		UNITS
		HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1) ($C_L = 15\text{ pF}$)	t_{PLH} t_{PHL}	8	11	ns
Power Dissipation Capacitance*	C_{PD}	26	38	pF

* C_{PD} is used to determine the dynamic power consumption, per gate.
 $PD = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency
 C_L = output load capacitance.
 V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input t_r , $t_f = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Input to Output (Fig. 1)	t_{PLH} t_{PHL}	2 4.5 6	— — —	100 20 17	— — —	— 28 —	— — —	125 25 21	— — —	— 35 —	— — —	150 30 26	— — —	— 42 —	ns
Transition Times (Fig. 1)	t_{TLH} t_{THL}	2 4.5 6	— — —	75 15 13	— — —	— 15 —	— — —	95 19 16	— — —	— 19 —	— — —	110 22 19	— — —	— 22 —	ns
Input Capacitance	C_i	—	—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_s	50% V_{CC}	1.3V

Fig. 1 — Transition times and propagation delay times.