

**PC74HC/HCT73**  
flip-flops

**DUAL JK FLIP-FLOP WITH RESET; NEGATIVE-EDGE TRIGGER**

**FEATURES**

- Output capability: standard
- I<sub>CC</sub> category: flip-flops

**GENERAL DESCRIPTION**

The 74HC/HCT73 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT73 are dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock ( $\overline{nCP}$ ) and reset ( $\overline{nR}$ ) inputs; also complementary Q and  $\overline{Q}$  outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ( $\overline{nR}$ ) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the  $\overline{Q}$  output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\overline{CP}$ to n $\overline{Q}$ n $\overline{CP}$ to n $\overline{Q}$ n $\overline{R}$ to n $\overline{Q}$ , n $\overline{Q}$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	17	19	ns
			15	18	ns
			14	17	ns
f <sub>max</sub>	maximum clock frequency		58	50	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	notes 1 and 2	30	30	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. C<sub>PD</sub> is used to determine the dynamic power-dissipation (P<sub>D</sub> in  $\mu$ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

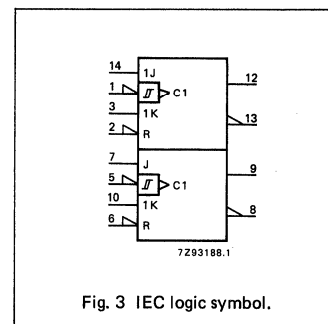
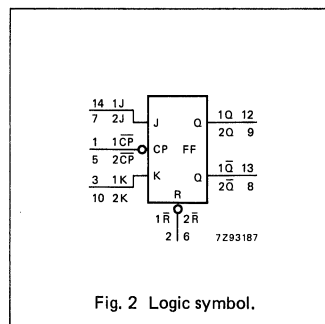
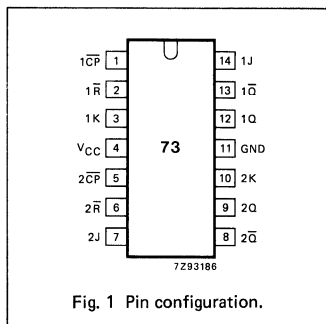
**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT73P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT73T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5	1 $\overline{CP}$ , 2 $\overline{CP}$	clock input (LOW-to-HIGH, edge-triggered)
2, 6	1 $\overline{R}$ , 2 $\overline{R}$	asynchronous reset inputs (active LOW)
4	V <sub>CC</sub>	positive supply voltage
11	GND	ground (0 V)
12, 9	1Q, 2Q	true flip-flop outputs
13, 8	1 $\overline{Q}$ , 2 $\overline{Q}$	complement flip-flop outputs
14, 7, 3, 10	1J, 2J, 1K, 2K	synchronous inputs; flip-flops 1 and 2



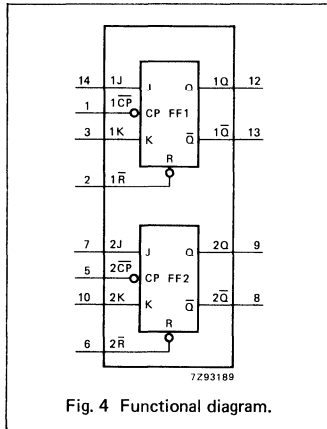


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	nR	nCP	J	K	Q	Q̄
asynchronous reset	L	X	X	X	L	H
toggle	H	↓	h	h	q̄	q
load "0" (reset)	H	↓	l	h	L	H
load "1" (set)	H	↓	h	l	H	L
hold "no change"	H	↓	l	l	q	q

H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition  
 X = don't care  
 ↓ = HIGH-to-LOW CP transition

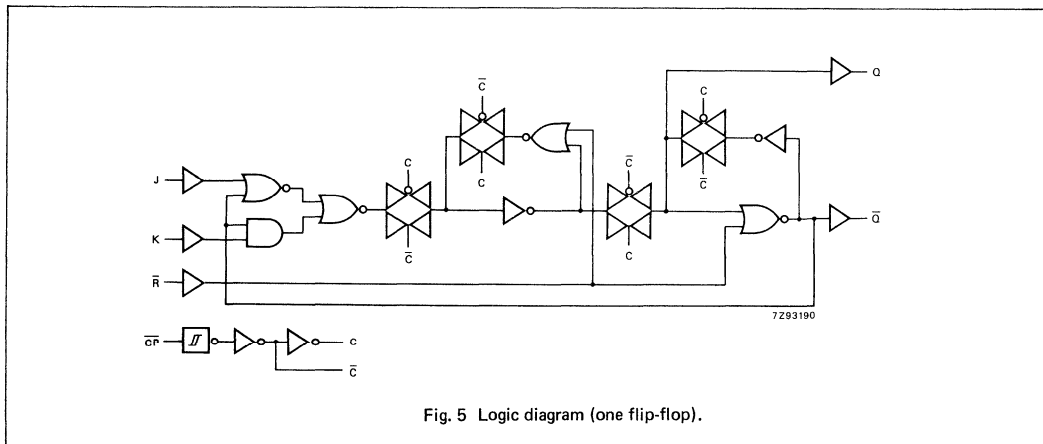


Fig. 5 Logic diagram (one flip-flop).

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: flip-flops

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ̄		50 18 14	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nR̄ to nQ, nQ̄		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	reset pulse width HIGH or LOW	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t <sub>rem</sub>	removal time nR̄ to nCP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	
t <sub>su</sub>	set-up time nJ, nK to nCP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>h</sub>	hold time nJ, nK to nCP	4 4 4	-3 -1 -1		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 6
f <sub>max</sub>	maximum maximum clock pulse frequency	6.0 30 35	18 54 64		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: flip-flops

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
nJ, nK	0.35
n $\bar{R}$	0.35
n $\bar{CP}$	0.35

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74 HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\bar{CP}$ to nQ		22	38		48		57	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\bar{CP}$ to n $\bar{Q}$		21	36		45		54	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\bar{R}$ to nQ, n $\bar{Q}$		20	34		43		51	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	23	12		29		35		ns	4.5	Fig. 6
t <sub>W</sub>	reset pulse width HIGH or LOW	18	9		23		27		ns	4.5	Fig. 7
t <sub>rem</sub>	removal time n $\bar{R}$ to n $\bar{CP}$	12	5		15		18		ns	4.5	
t <sub>su</sub>	set-up time nJ, nK to n $\bar{CP}$	12	5		15		18		ns	4.5	Fig. 6
t <sub>h</sub>	hold time nJ, nK to n $\bar{CP}$	5	0		5		5		ns	4.5	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	27	46		22		18		MHz	4.5	Fig. 6

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AC WAVEFORMS

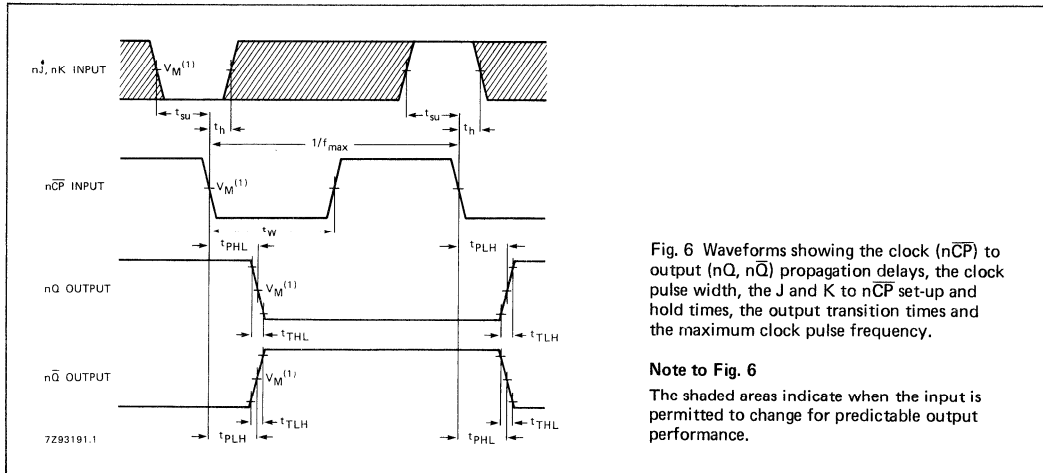


Fig. 6 Waveforms showing the clock ( $n\overline{CP}$ ) to output ( $nQ, n\overline{Q}$ ) propagation delays, the clock pulse width, the J and K to  $n\overline{CP}$  set-up and hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

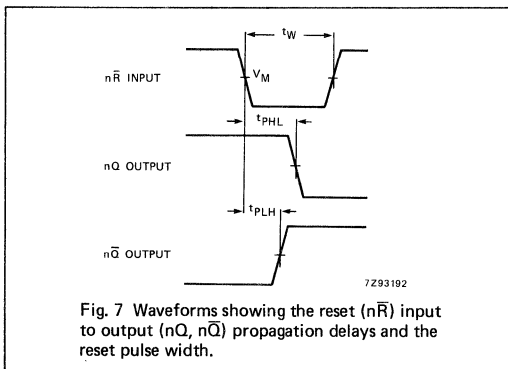


Fig. 7 Waveforms showing the reset ( $n\overline{R}$ ) input to output ( $nQ, n\overline{Q}$ ) propagation delays and the reset pulse width.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .