

MITSUBISHI LSSTLs
M74LS85P

4-BIT MAGNITUDE COMPARATOR

DESCRIPTION

The M74LS85P is a semiconductor integrated circuit containing a 4-bit digital comparator.

FEATURES

- Easy expansion of number of bits
- Binary or BCD comparison
- Wide operating temperature range ($T_a = -20 \sim +75^\circ C$)

APPLICATION

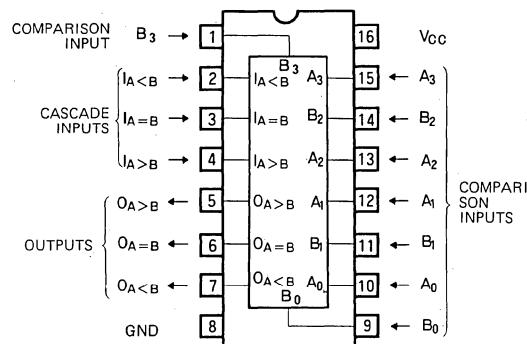
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

By applying two sets of 4-bit binary numbers A and B to be compared to comparison inputs $A_0 \sim A_3$ and $B_0 \sim B_3$ and by setting cascade input $I_{A=B}$ high, high appears in outputs $O_{A>B}$, $O_{A=B}$ and $O_{A<B}$ in accordance with the magnitude. This is used for connecting cascade inputs $I_{A>B}$, $I_{A<B}$ and $I_{A=B}$ and increasing the number of bits.

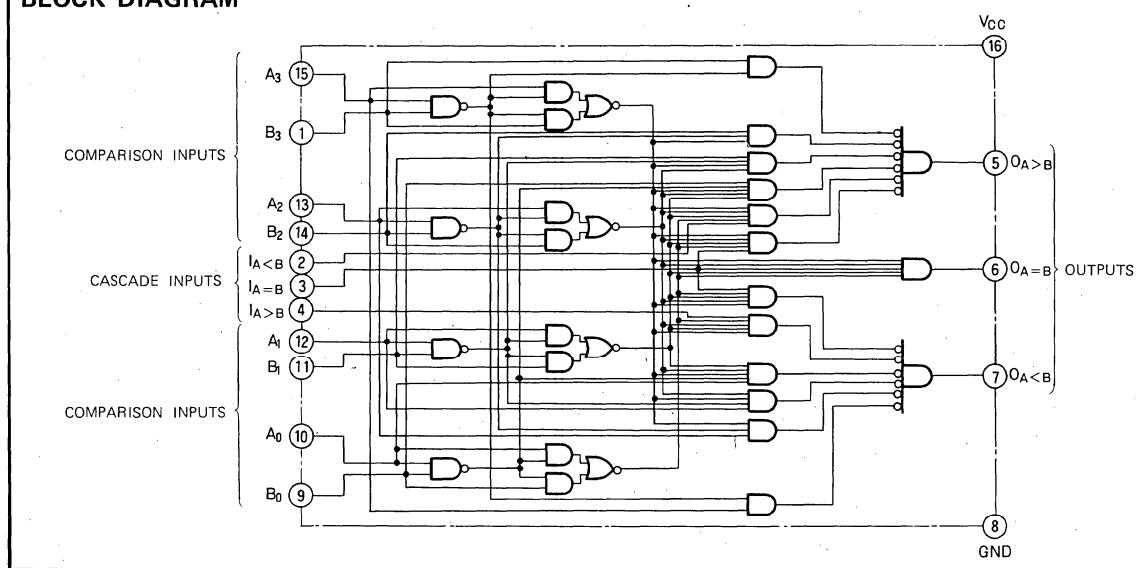
(Refer to application example)

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



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FUNCTION TABLE (Note 1)

A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	L	L

Note 1. X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions			Limits	Unit
		Min	Typ	Max		
V _{CC}	Supply voltage				-0.5 ~ +7	V
V _I	Input voltage				-0.5 ~ +15	V
V _O	Output voltage	High-level state			-0.5 ~ V _{CC}	V
Topr	Operating free-air ambient temperature range				-20 ~ +75	°C
T _{stg}	Storage temperature range				-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	4.75	5	5.25	V
I _{OH}	High-level output current	$V_{OH} \geq 2.7\text{V}$	0	-400	μA
I _{OL}	Low-level output current	$V_{OL} \leq 0.4\text{V}$	0	4	mA
		$V_{OL} \leq 0.5\text{V}$	0	8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits	Unit
		Min	Typ	Max		
V _{IH}	High-level input voltage				2	V
V _{IL}	Low-level input voltage				0.8	V
V _{IC}	Input clamp voltage	$V_{CC} = 4.75\text{V}, I_{IC} = -18\text{mA}$			-1.5	V
V _{OH}	High-level output voltage	$V_{CC} = 4.75\text{V}, V_I = 0.8\text{V}$ $V_I = 2\text{V}, I_{OH} = -400\mu\text{A}$			2.7	3.4
V _{OL}	Low-level output voltage	$V_{CC} = 4.75\text{V}$	$I_{OL} = 4\text{mA}$		0.25	0.4
		$V_I = 0.8\text{V}, V_I = 2\text{V}$	$I_{OL} = 8\text{mA}$		0.35	0.5
I _{IH}	High-level input current	$I_{A<B}, I_{A>B}$	$V_{CC} = 5.25\text{V}$			
		$A_0 \sim A_3, B_0 \sim B_3, I_{A=B}$	$V_I = 2.7\text{V}$			
		$I_{A<B}, I_{A>B}$	$V_{CC} = 5.25\text{V}$			
		$A_0 \sim A_3, B_0 \sim B_3, I_{A=B}$	$V_I = 10\text{V}$		0.1	mA
I _{IL}	Low-level input current	$I_{A<B}, I_{A>B}$	$V_{CC} = 5.25\text{V}$			
		$A_0 \sim A_3, B_0 \sim B_3, I_{A=B}$	$V_I = 0.4\text{V}$		-0.4	mA
I _{OS}	Short-circuit output current (Note 2)	$V_{CC} = 5.25\text{V}, V_O = 0\text{V}$			-20	-100
I _{CC}	Supply current	$V_{CC} = 5.25\text{V}$ (Note 3)			11	20

* : All typical values are at $V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$.

Note 2: All measurements must be done quickly and not more than output should be shorted at a time.

Note 3: I_{CC} is measured with $I_{A=B}$ at 0V and with all other inputs at 4.5V.

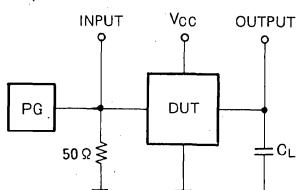
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SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^\circ C$, unless otherwise noted)

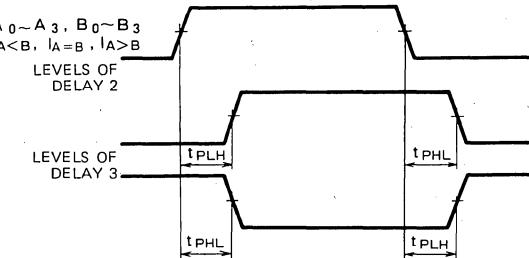
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Number of delay gate steps 1		6			ns
t_{PHL}	Number of delay gate steps 2		11			ns
t_{PLH}	Number of delay gate steps 3		10			ns
t_{PHL}	Number of delay gate steps 4		18			ns
t_{PLH}	Number of delay gate steps 5		12	36		ns
t_{PHL}	Number of delay gate steps 6		20	30		ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $A_0 \sim A_3, B_0 \sim B_3$ to outputs $O_A < B, O_A = B, O_A > B$	$C_L = 15\text{pF}$ (Note 4)	16	45		ns
t_{PHL}	Low-to-high-level, high-to-low-level output propagation time, from inputs $A_0 \sim A_3, B_0 \sim B_3$ to outputs $O_A < B, O_A = B, O_A > B$		20	45		ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $I_A = B$ to outputs $O_A < B, O_A = B$		6	22		ns
t_{PHL}	Low-to-high-level, high-to-low-level output propagation time, from input $I_A = B$ to output $O_A = B$		12	17		ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $I_A < B, I_A > B$ to outputs $O_A < B, O_A = B, O_A > B$		7	20		ns
t_{PHL}	Low-to-high-level, high-to-low-level output propagation time, from inputs $I_A < B, I_A > B$ to outputs $O_A < B, O_A = B, O_A > B$		13	26		ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $I_A < B, I_A > B$ to outputs $O_A < B, O_A = B, O_A > B$		9	22		ns
t_{PHL}	Low-to-high-level, high-to-low-level output propagation time, from inputs $I_A < B, I_A > B$ to outputs $O_A < B, O_A = B, O_A > B$		15	17		ns

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics:
 $PRR = 1\text{MHz}, t_r = 6\text{ns}, t_f = 6\text{ns}, t_w = 500\text{ns}, V_p = 3\text{Vp-p}, Z_0 = 50\Omega$.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

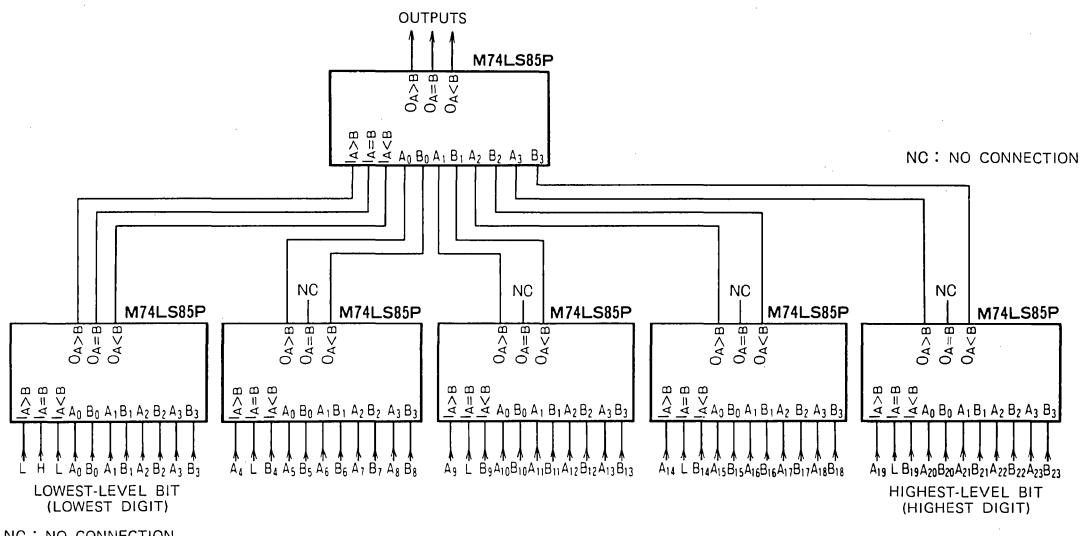


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APPLICATION EXAMPLES

- (1) Shown below is a 24-bit (digital) comparator using the M74LS85P. Expansion is possible up to n bits using this type of cascade connection.



- (2) Shown below is an n-bit comparator using the M74LS85P. The speed is decreases as the number of bits in the configuration below increases. configuration below.

