

General Description

This planar stripe MOSFET has better characteristics, such as fast switching time, fast reverse recovery time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for electronic ballast and switching mode power supplies.

FEATURES

- $V_{DSS} = 500V$, $I_D = 5.0A$
- Drain-Source ON Resistance : $R_{DS(ON)} = 1.4$ @ $V_{GS} = 10V$
- $Q_g(\text{typ}) = 12nC$
- $t_{rr(\text{typ})} = 150ns$

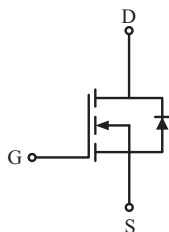
MAXIMUM RATING (Tc=25)

| CHARACTERISTIC | SYMBOL | RATING | | UNIT | |
|---|-----------------|----------------------|----------------------|------|----|
| | | KF5N50PR KF5N50PS | KF5N50FR KF5N50FS | | |
| Drain-Source Voltage | V_{DSS} | 500 | | V | |
| Gate-Source Voltage | V_{GSS} | ± 30 | | V | |
| Drain Current | @ $T_C = 25$ | I_D | 5.0 | 5.0* | A |
| | @ $T_C = 100$ | | 2.9 | 2.9* | |
| | Pulsed (Note1) | | I_{DP} | 13 | |
| Single Pulsed Avalanche Energy (Note 2) | E_{AS} | 270 | | mJ | |
| Repetitive Avalanche Energy (Note 1) | E_{AR} | 8.6 | | mJ | |
| Peak Diode Recovery dv/dt (Note 3) | dv/dt | 20 | | V/ns | |
| Drain Power Dissipation | Tc=25 | P_D | 83 | 41.5 | W |
| | Derate above 25 | | 0.66 | 0.33 | W/ |
| Maximum Junction Temperature | T_j | 150 | | | |
| Storage Temperature Range | T_{stg} | -55 150 | | | |
| Thermal Characteristics | | | | | |
| Thermal Resistance, Junction-to-Case | R_{thJC} | 1.5 | 3.0 | /W | |
| Thermal Resistance, Junction-to-Ambient | R_{thJA} | 62.5 | 62.5 | /W | |

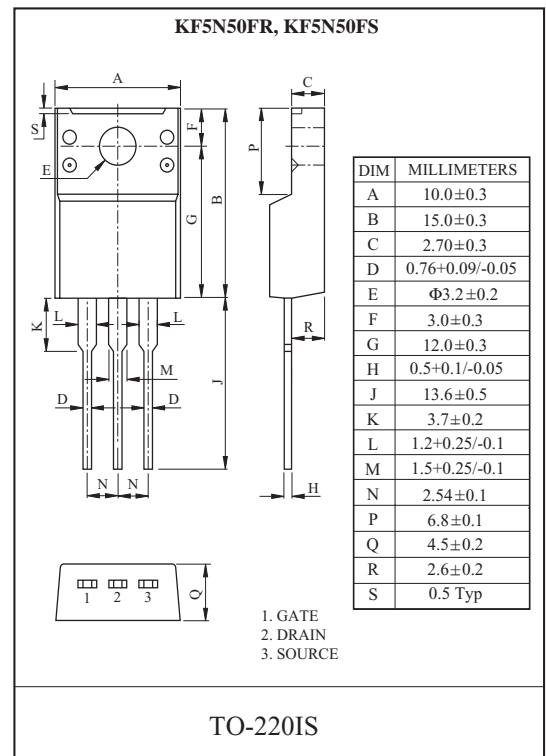
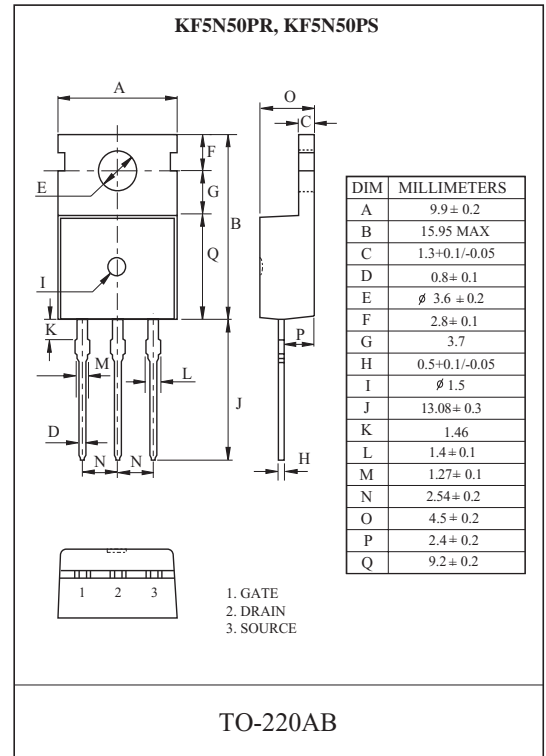
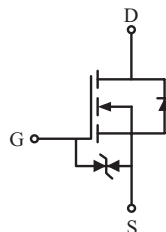
* : Drain current limited by maximum junction temperature.

PIN CONNECTION

(KF5N50PR, KF5N50FR)



(KF5N50PS, KF5N50FS)



KF5N50PR/FR/PS/FS

ELECTRICAL CHARACTERISTICS (Tc=25)

| CHARACTERISTIC | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|------------------------------------|---|------|------|-------|------|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | BV _{DSS} | I _D =250μA, V _{GS} =0V | 500 | - | - | V |
| Breakdown Voltage Temperature Coefficient | BV _{DSS} / T _j | I _D =250μA, Referenced to 25 | - | 0.55 | - | V/ |
| Drain Cut-off Current | I _{DSS} | V _{DS} =500V, V _{GS} =0V, | - | - | 10 | μA |
| Gate Threshold Voltage | V _{th} | V _{DS} =V _{GS} , I _D =250μA | 2.0 | - | 4.0 | V |
| Gate Leakage Current | I _{GSS} | KF5N50PR/FR V _{GS} = ± 30V, V _{DS} =0V | - | - | ± 100 | nA |
| | | KF5N50PS/FS V _{GS} = ± 25V, V _{DS} =0V | - | - | ± 10 | μA |
| Drain-Source ON Resistance | R _{DS(ON)} | V _{GS} =10V, I _D =2.5A | - | 1.15 | 1.4 | |
| Dynamic | | | | | | |
| Total Gate Charge | Q _g | V _{DS} =400V, I _D =5A V _{GS} =10V (Note4,5) | - | 12 | - | nC |
| Gate-Source Charge | Q _{gs} | | - | 2.4 | - | |
| Gate-Drain Charge | Q _{gd} | | - | 5.4 | - | |
| Turn-on Delay time | t _{d(on)} | V _{DD} =250V R _L =50 R _G =25 (Note4,5) | - | 22.5 | - | ns |
| Turn-on Rise time | t _r | | - | 29 | - | |
| Turn-off Delay time | t _{d(off)} | | - | 58 | - | |
| Turn-off Fall time | t _f | | - | 18 | - | |
| Input Capacitance | C _{iss} | V _{DS} =25V, V _{GS} =0V, f=1.0MHz | - | 430 | - | pF |
| Output Capacitance | C _{oss} | | - | 71 | - | |
| Reverse Transfer Capacitance | C _{rss} | | - | 7.5 | - | |
| Source-Drain Diode Ratings | | | | | | |
| Continuous Source Current | I _S | V _{GS} <V _{th} | - | - | 5 | A |
| Pulsed Source Current | I _{SP} | | - | - | 20 | |
| Diode Forward Voltage | V _{SD} | I _S =5A, V _{GS} =0V | - | - | 1.4 | V |
| Reverse Recovery Time | t _{rr} | I _S =5A, V _{GS} =0V, dI _S /dt=100A/μs | - | 150 | - | ns |
| Reverse Recovery Charge | Q _{rr} | | - | 0.42 | - | μC |

Note 1) Repetivity rating : Pulse width limited by junction temperature.

Note 2) L=19.5mH, I_S=5A, V_{DD}=50V, R_G=25 , Starting T_j=25 .

Note 3) I_S 5A, dI/dt 100A/μs, V_{DD} BV_{DSS}, Starting T_j=25 .

Note 4) Pulse Test : Pulse width 300μs, Duty Cycle 2%.

Note 5) Essentially independent of operating temperature.

Marking

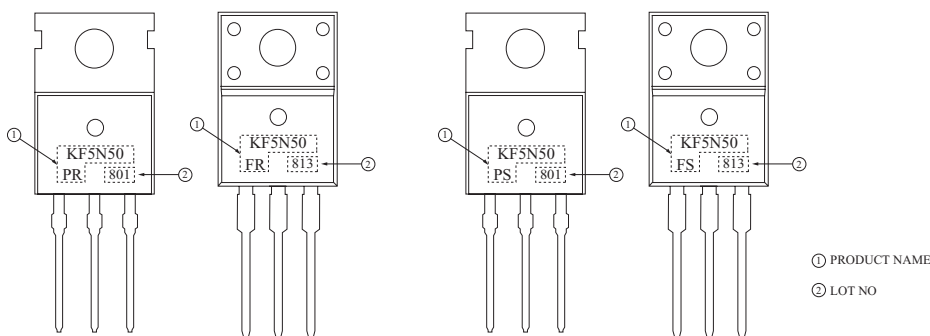


Fig1. $I_D - V_{DS}$

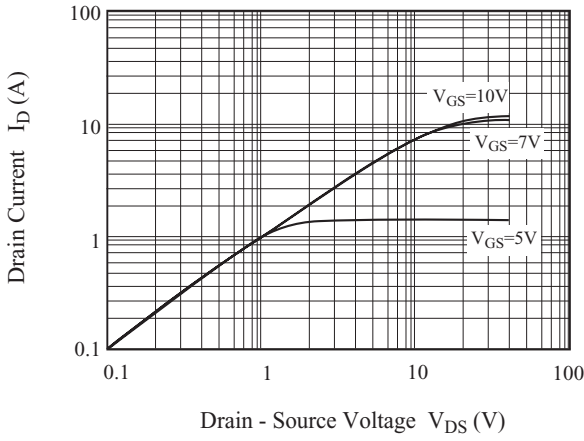


Fig2. $I_D - V_{GS}$

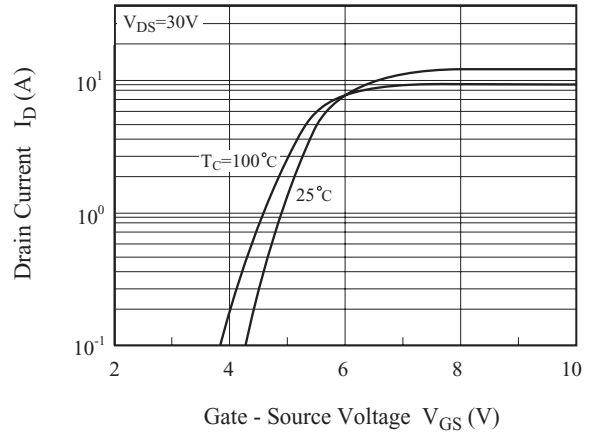


Fig3. $BV_{DSS} - T_j$

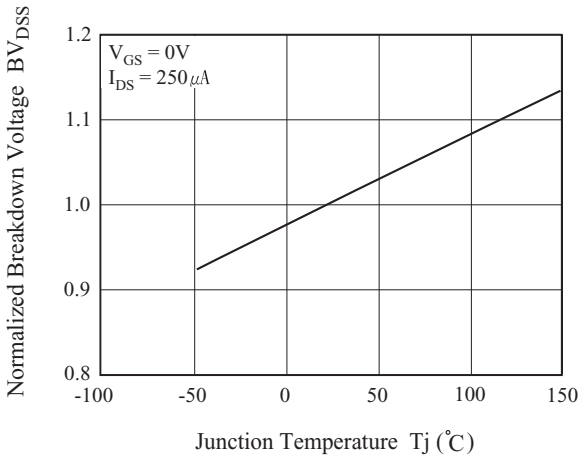


Fig4. $R_{DS(ON)} - I_D$

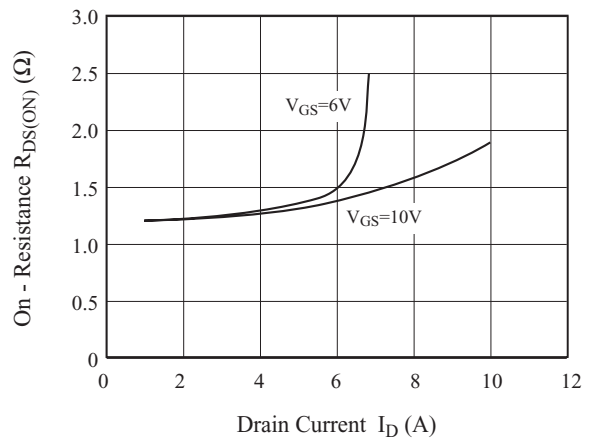


Fig5. $I_S - V_{SD}$

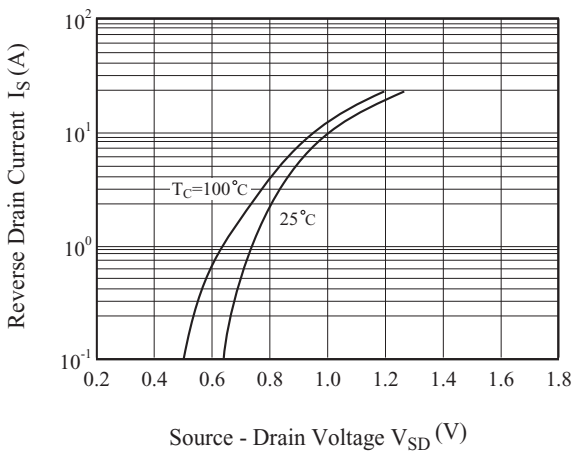
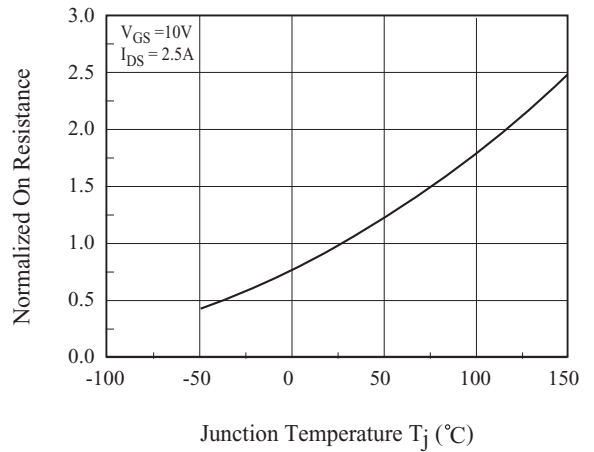


Fig6. $R_{DS(ON)} - T_j$



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Fig 7. C - V_{DS}

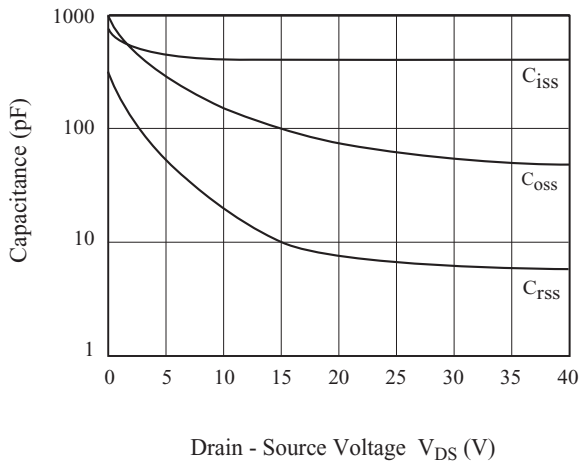


Fig8. Q_g- V_{GS}

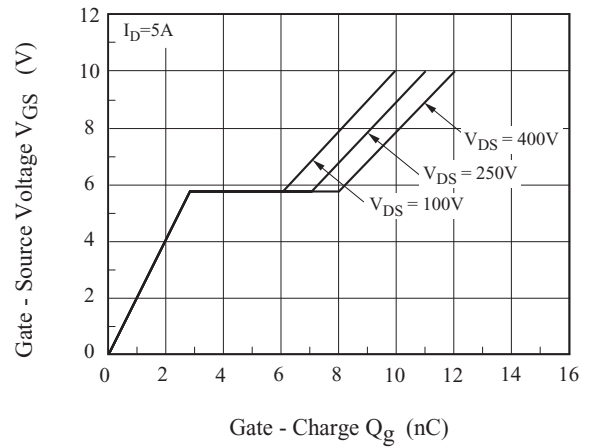


Fig9. Safe Operation Area

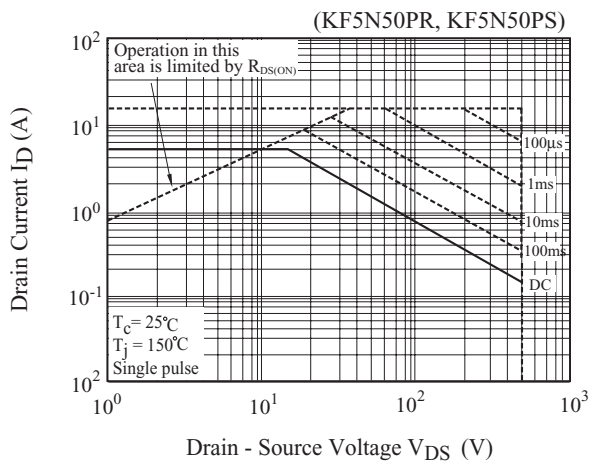


Fig10. Safe Operation Area

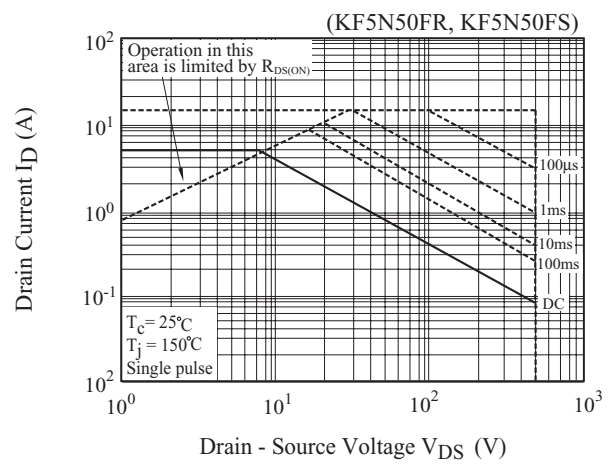
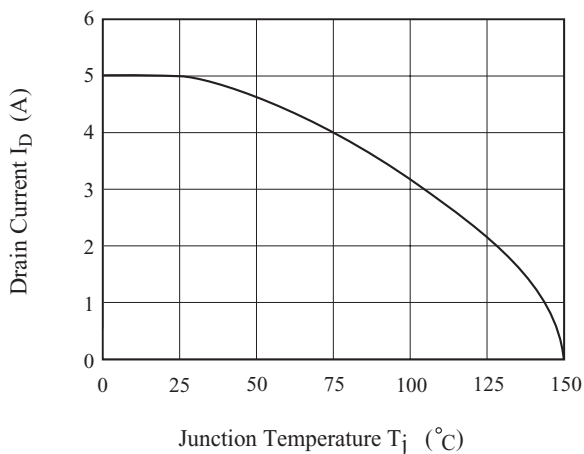


Fig11. I_D - T_j



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Fig12. Transient Thermal Response Curve

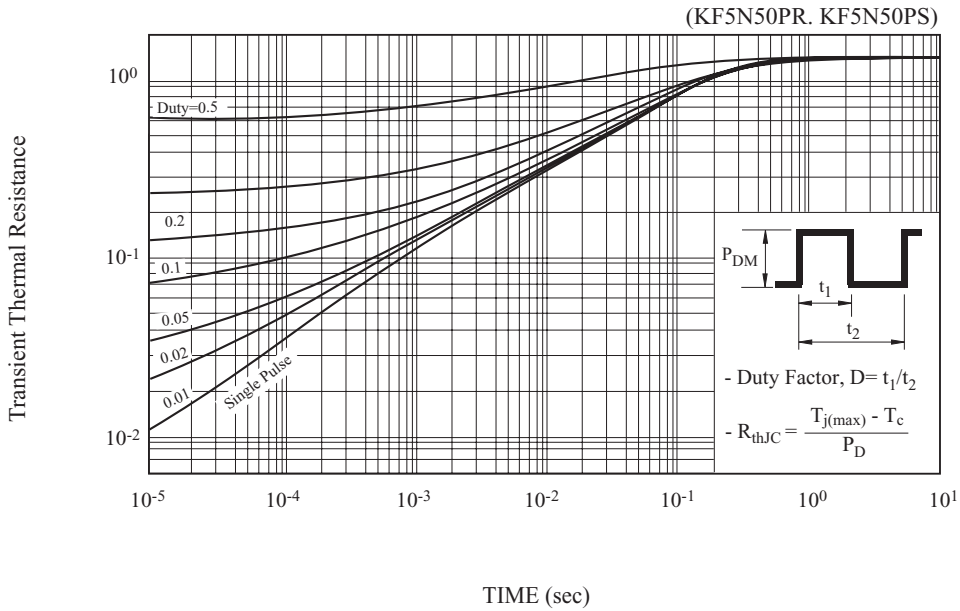


Fig13. Transient Thermal Response Curve

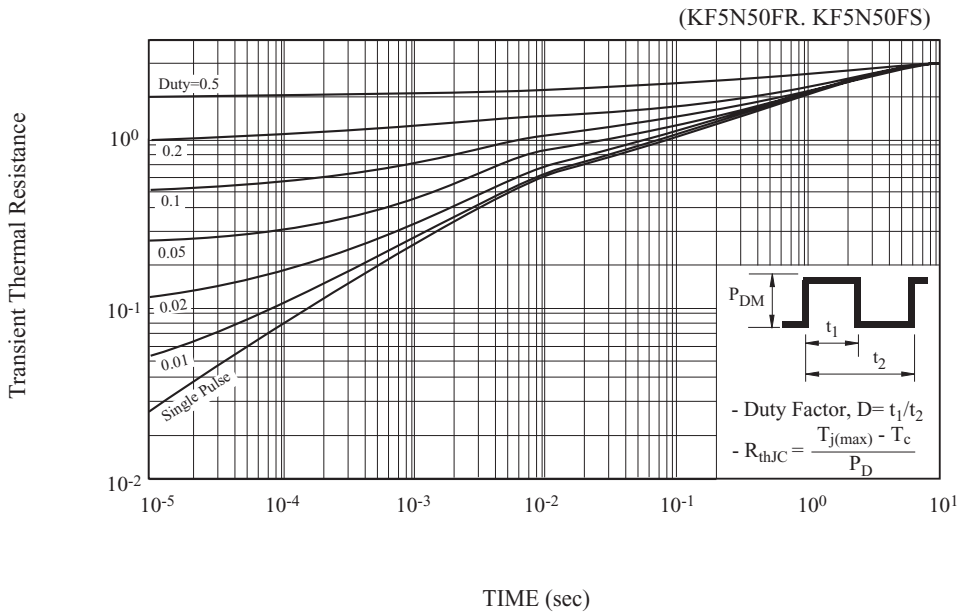


Fig14. Gate Charge

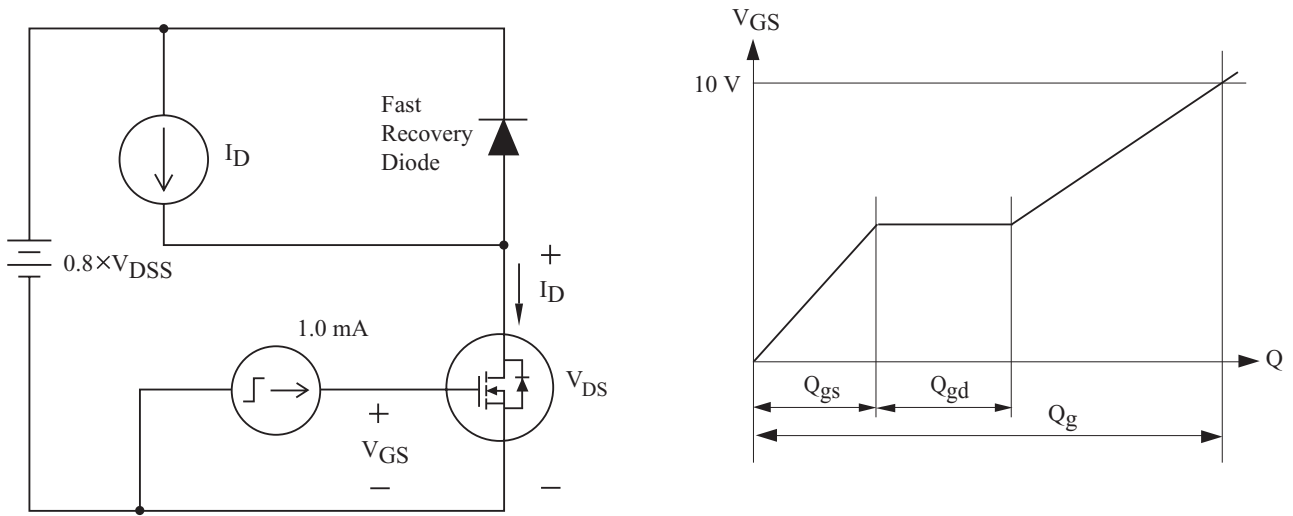


Fig15. Single Pulsed Avalanche Energy

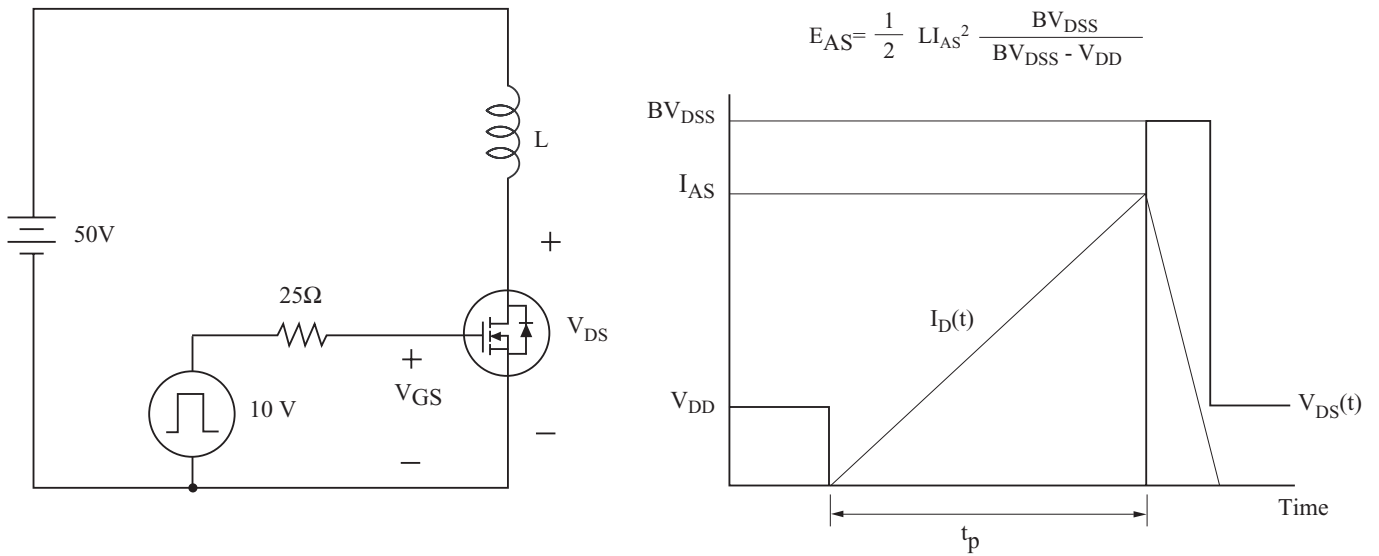


Fig16. Resistive Load Switching

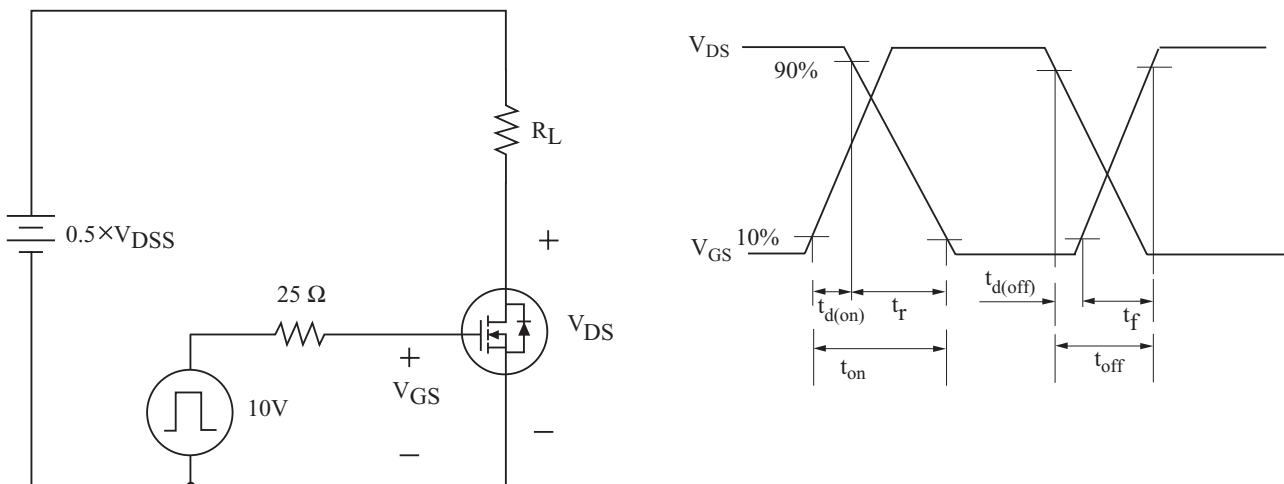


Fig17. Source - Drain Diode Reverse Recovery and dv/dt

