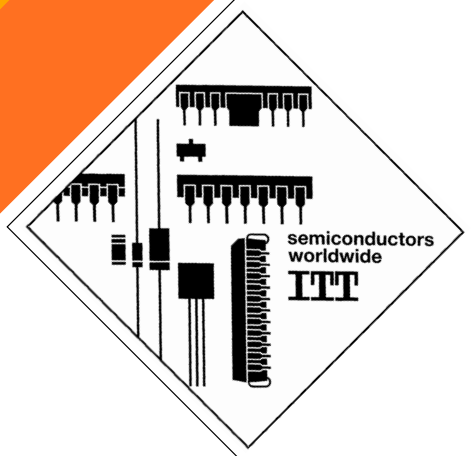

PIP 2250
Picture-in-Picture
Processor

Edition March 3, 1992
6251-283-5E

ITT Semiconductors

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Picture–in–Picture Processor

1. Introduction

The so–called picture–in–picture facility has been introduced for the first time by ITT in 1977, using the UAA 1000 and SAA 3000 integrated circuits. Picture–in–picture means the insertion of a second program's picture on the screen of a CTV receiver (at reduced size) simultaneously with the full–size main picture. The second small picture may originate from another TV transmitter, from a video recorder, a monitor camera or another source. It allows monitoring of the second channel while watching the main channel. Main requirement for picture–in–picture is to store the content of the small picture when it is supplied by its source, and to deliver the content at the proper instant when it must be inserted into the main picture which is received and displayed continuously.

In the past, at the first attempts of picture–in–picture, the memory for storing the content of the small picture was analog, a bucket brigade MOS device, according to the state of the art at this time. Today's state of the art is digital: ITT's DIGIT 2000 system with its digital processing of the video signals opens new possibilities for picture–in–picture which are only feasible in a digital system. For storing the content of the second, small picture, two standard 64 K dynamic RAMs (16 K x 4) are used, thus making the storage simple and economic. If it is intended to store up to four small pictures, two 256 K DRAMs (64 K x 4) are required. Page mode must be provided in both cases.

Today's picture–in–picture fits neatly into ITT's DIGIT 2000 system, but is also suitable for stand–alone applications.

1.1. General Description

The PIP 2250 Picture–in–Picture Processor is a fast signal processor in CMOS technology which is used to filter (for anti–aliasing) and to decimate the digital Y, R–Y and B–Y signals supplied, e.g., by the VSP 2860 Video/Sync Processor, to control the DRAMs for storing the small picture's content and for reading the same at the proper time for display. Further, a border generator supplies the borderline for the small picture. the PIP 2250 is housed in a 68–pin PLCC package, and is compatible to the DIGIT 2000 system of digital signal processors with respect to signal levels as well as pin configuration, supply voltage, clock frequency etc.

A coarse block diagram of the PIP 2250 is shown in Fig. 1–1. The input picture processing section receives the digitized information of the small, second picture to be inserted into the main picture, in the shape of the so–called input YUV bus, from the VSP 2860 Video Sync Processor or a similar source, together with the associated clock, skew, horizontal and vertical blanking signals. The DRAM interface gives the filtered and decimated YUV and sync information to the DRAM for storing till the proper instant for insertion into the main picture has come. At this time, the DRAM's content is read and processed in the output picture processing section, which receives its required clock, skew and blanking signals from the main system into whose picture the second small picture is intended to be inserted. The output picture processing section supplies the small picture's content in the shape of the output YUV bus, which is connected to the YUV bus supplied by the main picture's video processing section (Fig. 1–2). By means of the ODOUT Outputs Disable signal supplied by the PIP 2250 via pin 47, the main video section is disabled during the time of the small picture.

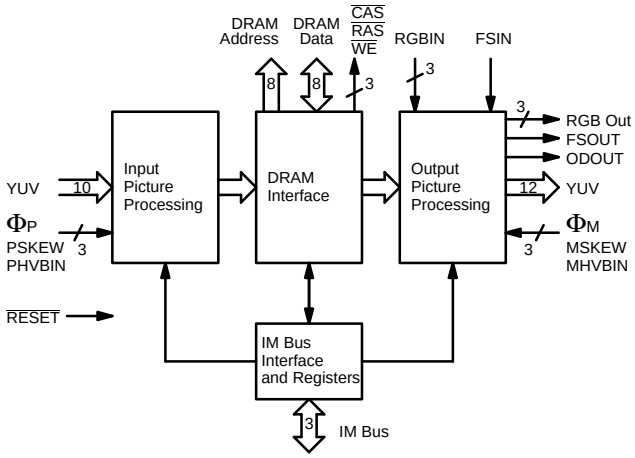

Fig. 1–1: PIP 2250 block diagram

1.2. Features

Main features of the PIP 2250 Picture–in–Picture Processor are

– digital video filters for anti–aliasing and data decimation

– control of the two DRAMs for storage of the small picture(s)

– control and supervision of the PIP 2250 via the IM bus

– full compatibility with the DIGIT 2000 system

1.3. Environment

The block diagram of the video section of a digital TV receiver according to the DIGIT 2000 concept, which is equipped with the picture–in–picture facility, is shown in Fig. 1–2. Besides the well known DIGIT 2000 chip set, shown in the upper part of Fig. 1–2, there is the section for the second (small) picture. This section is composed of the VAD 2150 Video A/D Converter, the VSP 2860 Video/Sync Processor, optionally a SECAM processor, the PIP 2250 Picture–in–Picture Processor and two DRAMs. The block diagram for the PIP 2250 standard operation is shown in Fig. 1–3.

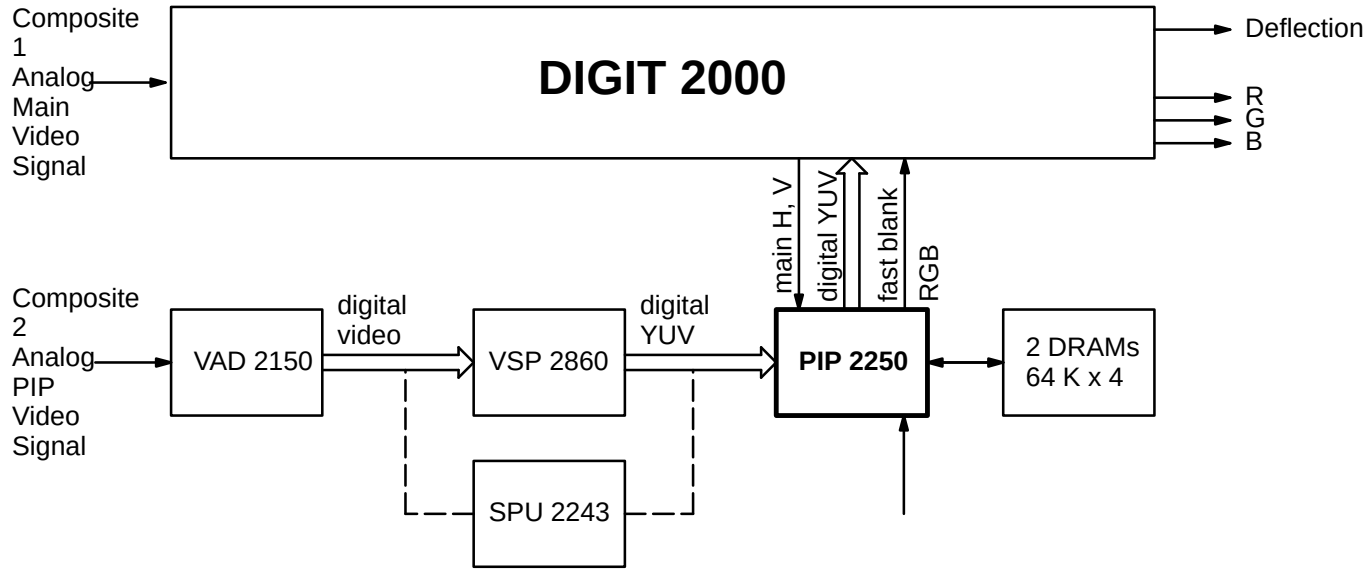

Fig. 1–2: Picture–in–picture block diagram (digital insertion)

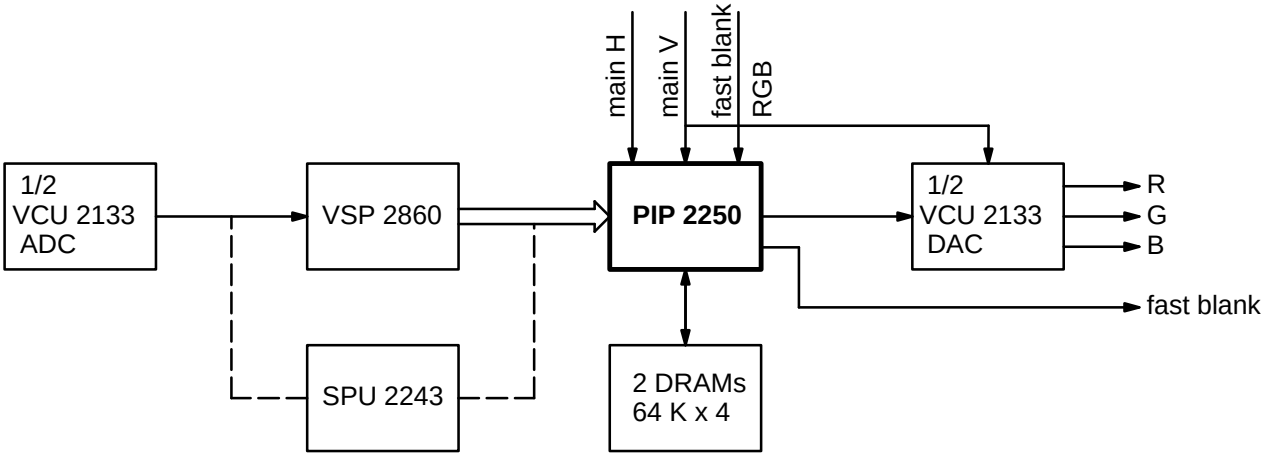

Fig. 1–3: Picture–in–picture block diagram (stand–alone operation)

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2. Specifications

2.1. Outline Dimensions

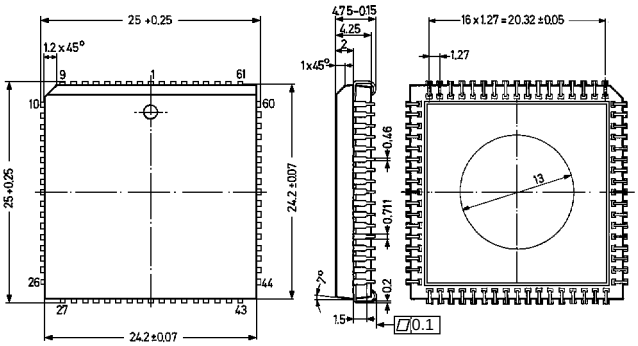

Fig. 2–1: PIP 2250 in 68–pin PLCC package

Weight approx. 4.5 g, Dimensions in mm

2.2. Pin Connections

Pin No.	Short Name	Full Pin Name	Output Type	Input Type
1	GND	Ground	–	–
2	A7	A7 RAM Address Output (MSB)	TTL	–
3	A6	A6 RAM Address Output	TTL	–
4	A5	A5 RAM Address Output	TTL	–
5	A4	A4 RAM Address Output	TTL	–
6	A3	A3 RAM Address Output	TTL	–
7	A2	A2 RAM Address Output	TTL	–
8	A1	A1 RAM Address Output	TTL	–
9	A0	A0 RAM Address Output (LSB)	TTL	–
10	IO7	IO7 RAM Data Input/Output (MSB)	TS TTL	TTL
11	IO6	IO6 RAM Data Input/Output	TS TTL	TTL
12	IO5	IO5 RAM Data Input/Output	TS TTL	TTL
13	IO4	IO4 RAM Data Input/Output	TS TTL	TTL
14	IO3	IO3 RAM Data Input/Output	TS TTL	TTL
15	IO2	IO2 RAM Data Input/Output	TS TTL	TTL
16	IO1	IO1 RAM Data Input/Output	TS TTL	TTL
17	IO0	IO0 RAM Data Input/Output (LSB)	TS TTL	TTL
18	V_{SUP}	V_{SUP} Supply Voltage	–	–
19	GND	Ground	–	–

Pin Connections, continued

Pin No.	Short Name	Full Pin Name	Output Type	Input Type
20	$\overline{\text{CAS}}$	CAS Column Address Strobe Output	TTL	–
21	$\overline{\text{RAS}}$	RAS Row Address Strobe Output	TTL	–
22	$\overline{\text{WE}}$	WE Write Enable Output	TTL	–
23	FSIN	FSIN Fast Switching Input	–	TTL
24	RIN	R Analog Input	–	Analog
25	GIN	G Analog Input	–	Analog
26	BIN	B Analog Input	–	Analog
27	BOUT	B Analog Output	Analog	–
28	GOUT	G Analog Output	Analog	–
29	ROUT	R Analog Output	Analog	–
30	FSOUT	FSOUT Fast Switching Output	TTL	–
31	C0	C0 Chroma Output (LSB) and Mysnc Input	OD YUV	YUV
32	C3	C3 Chroma Output (MSB)	OD YUV	–
33	C2	C2 Chroma Output	OD YUV	–
34	C1	C1 Chroma Output	OD YUV	–
35	$\overline{\text{RESET}}$	Reset Input	–	RESET
36	L0	L0 Luma Output (LSB)	OD YUV	–
37	L2	L1 Luma Output	OD YUV	–
38	L3	L2 Luma Output	OD YUV	–
39	L4	L3 Luma Output	OD YUV	–
40	L4	L4 Luma Output	OD YUV	–
41	L5	L5 Luma Output	OD YUV	–
42	L6	L6 Luma Output	OD YUV	–
43	L7	L7 Luma Output (MSB)	OD YUV	–
44	MSKEW or MHBL	Main System’s Skew Data Input (digital insertion) Main Horizontal Blank Input (stand–alone)	–	YUV
45	MHVBIN	MHVBIN Main System’s Vertical and Delayed Horizontal Blanking Pulse Input	–	Sandcastle
46	IMPORT	IM Bus Port Output	TTL	–
47	ODOUT	ODOUT Outputs Disable Output	TS TTL	–
48	BLC	Blocking Capacitor	–	–

Pin Connections, continued

Pin No.	Short Name	Full Pin Name	Output Type	Input Type
49	V_{SUP}	V_{SUP} Supply Voltage	–	–
50	ΦM	ΦM Main Clock Input	–	Clock
51	GND	Ground	–	–
52	Ident	IM Bus Ident Input	–	IMB
53	Clock	IM Bus Clock Input	–	IMB
54	Data	IM Bus Data Input/Output	OD IMB	IMB
55	PHVBIN	PHVBIN PIP System's Vertical and Delayed Horizontal Blanking Pulse Input	–	Sandcastle
56	PSKEW	PIP System's Skew Data Input	–	YUV
57	L7	L7 Luma Input (MSB)	–	YUV
58	L6	L6 Luma Input	–	YUV
59	L5	L5 Luma Input	–	YUV
60	L4	L4 Luma Input	–	YUV
61	L3	L3 Luma Input	–	YUV
62	L2	L2 Luma Input (LSB)	–	YUV
63	C1	C1 Chroma Input	–	YUV
64	C2	C2 Chroma Input	–	YUV
65	C3	C3 Chroma Input (MSB)	–	YUV
66	C0	C0 Chroma Input (LSB)	–	YUV
67	V_{SUP}	V_{SUP} Supply Voltage	–	–
68	ΦP	ΦP PIP Clock Input	–	Clock

Notes:
TTL = TTL Levels
OD TTL = open–drain TTL configuration
TS TTL = tristate TTL levels
YUV = fast YUV bus levels
OD YUV = open–drain YUV configuration
IMB = IM bus
Sandcastle = two different pulses are transferred via one line as described in the DPU's data sheet
Clock = the fast ΦM or ΦP clocks are fed to these pins

2.3. Pin Descriptions

Pins 1, 19 and 51 – Ground
These pins must be connected to the negative of the supply.

Pins 2 to 9 – A7 to A0 RAM Address Outputs (Fig. 2–11)
By means of these outputs, the external DRAMs are addressed.

Pins 10 to 17 – IO7 to IO0 RAM Data Inputs/Outputs (Fig. 2–8)
When writing the DRAMs, these pins are the data outputs, and when reading the DRAMs, they act as data input.

Pins 18, 49 and 67 – V_{SUP} Supply Voltage
This pins must be connected to the positive of the supply.

Pin 20 – $\overline{CAS}$ Column Address Strobe Output (Fig. 2–11)
This output supplies the column address strobe signal for the external DRAMs.

Pin 21 – $\overline{RAS}$ Row address Strobe Output (Fig. 2–11)
This output supplies the row address strobe signal for the external DRAMs.

Pin 22 – $\overline{WE}$ Write enable Output (Fig. 2–11)
This output supplies the write enable signal for the external DRAMs

Pin 23 – FSIN Fast Switching Input (Fig. 2–2)
This input serves for enabling the analog RGB inputs.

Pins 24 to 26 – Analog RGB Inputs (Fig. 2–12)
Via these inputs, the PIP 250 receives analog RGB signals, e.g. Teletext or video recorder (SCART), which are fed to the analog RGB outputs to be given to the VCU.

Pins 27 to 29 – Analog RGB Outputs (Fig. 2–12)
these outputs either supply the analog RGB signals, which have been received via the analog RGB input pins 24 to 26, to the VCU, or are the digital outputs for the analog border (with CMOS level).

Pin 30 – FSOUT Fast Switching Output (Fig. 2–11)
This output supplies a switching signal for enabling the analog RGB inputs of the VCU.

Pin 31 – C0 Chroma Output and Msync Input (Fig. 2–9)
This input/output, which, in its output function, can be disabled by the CCU via the IM bus, on the one hand supplies the LSB of the (R–Y) and (B–Y) digital color difference signals, which are multiplexed on four lines, to the VCU Video Codec for D/A conversion. On the other hand, pin 31 acts as input for the Msync multiplex sync signal when operating in the digital insertion mode.

Pins 32 to 34 – C1 to C3 chroma Outputs (Fig. 2–13)
These open–drain outputs, which can be disabled by the CCU via the IM bus, supply the three LSBs of the (R–Y) and (B–Y) digital color difference signals multiplexed on four lines to the VCU Video Codec for D/A conversion.

Pin 35 – $\overline{Reset}$ Input (Fig. 2–3)
This input is used for hardware reset of the PIP 2250. At Low level, reset is actuated, and at High level, the PIP is ready for communication with the CCU.

Pins 36 to 43 – L0 to L7 Luma Outputs (Fig. 2–13)
These open–drain outputs which can be disabled by the CCU via the IM bus, deliver the processed luminance signal in a parallel 8–bit code to the VCU Video Codec for D/A conversion.

Pin 44 – MSKEW Skew Data Input for digital insertion (Fig. 2–4)
Via this pin the PIP 2250 receives skew data for phase adjustment of the video information, from the DPU 2553 or DPU 2554 Deflection Processor of the Main system.
or
MHBL Horizontal Blank Input for stand–alone operation
This signal is used internally for horizontal start and for skew data measurement.

Pin 45 – MHVBIN Horizontal and Vertical blanking Pulse Input for Main System or Vertical Blanking Pulse Input for Stand–Alone Systems (Fig. 2–5).
Via pin 45, the PIP 2250 is supplied with the (sandcastled) delayed horizontal and vertical blanking pulses by pin 22 of the DPU 2553 or DPU 2554 Deflection Processor of the Main system, or, with stand–alone solutions, with the vertical blanking pulse of the Main system.

Pin 46 – IM Bus Port Output (Fig. 2–11)
The output level of this pin can be defined via the IM bus using bit 3 in address 57.

Pin 47 – ODOUT VPU Outputs Disable Output (Fig. 2–11)
This output must be connected to the outputs disable input of the PVPU or CVPU Video Processor acting together with the picture–in–picture system, in order to disable the main picture during the time the second small picture is displayed. The output signal of pin 47 has High level during the time the VPU's outputs must be disabled. During this time, the PIP's luma and chroma outputs are enabled. Vice versa, if pin 47 supplies Low level, the PIP's outputs are disabled and the VPU's luma and chroma outputs are enabled.

Pin 48 – Blocking Capacitor
for analog skew data measurement and analog delay of RGB output, ODOUT and FSOUT.

Pin 50 – ΦM Clock Input (Fig. 2–6)
This pin receives the ΦM main clock signal for the main picture from the MCU 2600 or MCU 2632 Clock Generator.

Pins 52 to 54 – IM Bus Connections (Figs. 2–3 and 2–10)
Via these pins, the PIP 2250 is connected to the IM bus and communicates with the CCU.

Pin 55 – PHVBIN Horizontal and Vertical Blanking Pulse Input from PIP System (Fig. 2–5)
Via pin 55, the PIP 2250 is supplied with the (sandcastled) delayed horizontal and vertical blanking pulses by the VSP 2860 Video/Sync Processor of the PIP system or another suitable source.

Pin 56 – PSKEW Skew Data Input from PIP System (Fig. 2–7)
Via pin 56, the PIP 2250 receives skew data for phase adjustment of the video information, from the VSP 2860 Video/Sync Processor of the PIP system or another suitable source.

Pins 57 to 66 – L7 to L2 and C3 to C0 Luma and Chroma inputs (Fig. 2–7)
Via these inputs, the PIP 2250 receives the digital luma and chroma signals for the PIP small picture for the VSP 2860 Video/Sync Processor or another suitable source. The luma signals are parallel in a 6–bit code, the chroma signals in the shape (R–Y) and (B–Y), time multiplexed on four lines.

Pin 68 – ΦP Clock Input (Fig. 2–6)
Via pin 68, the PIP 2250 receives the ΦP clock signal required for the PIP small picture, form the VSP 2860 Video/Sync Processor or another suitable source.

2.4. Pin Circuits

The following figures show schematically the circuitry at the various pins. The integrated protection structures are not shown. The letter “N” means N–channel, the letter “P” P–channel, both enhancement mode.

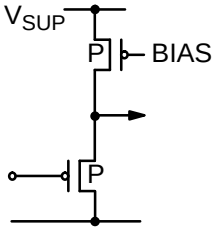

Fig. 2–2:
Input Pin 23

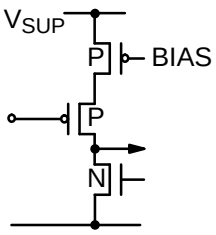

Fig. 2–3:
Input Pins 35, 52 and 53

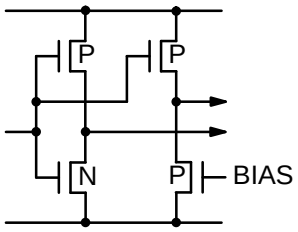

Fig. 2–4:
Input Pin 44

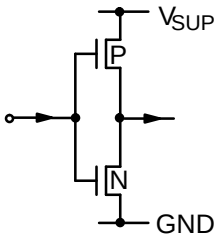

Fig. 2–5:
Input Pins 45 and 55

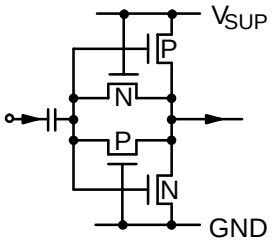

Fig. 2–6:
Input Pins 50 and 68

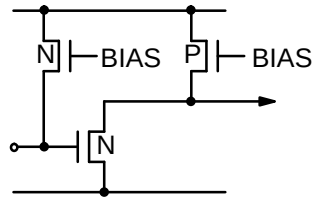

Fig. 2–7:
Input Pins 56 to 66

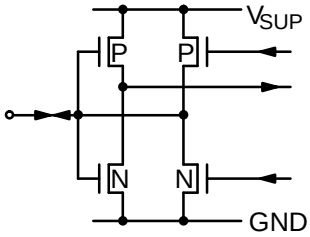

Fig. 2–8:
Input/Output Pins 10 to 17

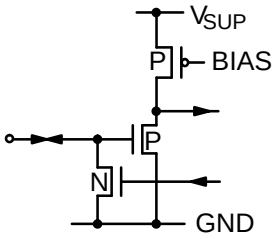

Fig. 2–9:
Input/Output Pin 31

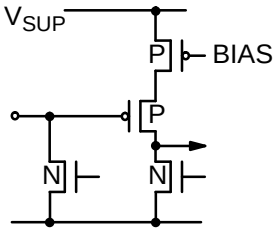

Fig. 2–10:
Input/Output Pin 54

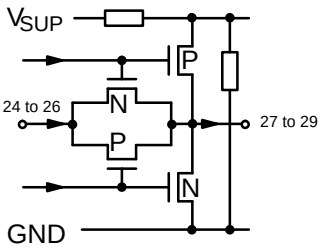

Fig. 2–12:
Input Pins 24 to 26,
Output Pins 27 to 29

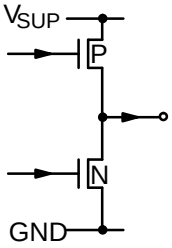

Fig. 2–11:
Output Pins 2 to 9,
20 to 22, 30, 46 and 47

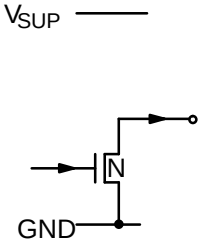

Fig. 2–13:
Output Pins 32 to 34 and
36 to 43

2.5. Electrical Characteristics

All voltages are referred to ground.

2.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	–40	+125	°C
V_{SUP}	Supply Voltage	18, 49,67	–	6	V
V_I	Input Voltage, all Inputs	–	–0.3 V	V_{SUP}	–
V_O	Output Voltage, all Outputs	–	–0.3 V	V_{SUP}	–
I_O	Output Current, all Push–Pull Outputs	–	–10	+10	mA
I_O	Output Current, all Open–Drain Outputs	–	–	+10	mA

2.5.2. Recommended Operating Conditions at T_A = 0 to 65 °C, $f_{\Phi M}$ = 14.3 to 20.25 MHz, $f_{\Phi P}$ = 14.3 to 20.25 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	18, 49, 67	4.75	5.0	5.25	V
$V_{\Phi MIDC}$	ΦM Clock Input D.C. Voltage	50	1.5	–	3.5	V
$V_{\Phi MIAC}$	ΦM Clock Input A.C. Voltage (p–p)		0.8	–	2.5	V
$\frac{t_{\Phi MIH}}{t_{\Phi MIL}}$	ΦM Clock Input High/Low Ratio		0.9	1.0	1.1	–
$t_{\Phi MIHL}$	ΦM Clock Input High to Low Transition Time		–	–	$\frac{0.15}{f_{\Phi M}}$	–

Recommended Operating Connections, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
$V_{\Phi PIDC}$	ΦP Clock Input D.C. Voltage	68	1.5	–	3.5	V
$V_{\Phi PIAC}$	ΦP Clock Input A.C. Voltage (p–p)		0.8	–	2.5	V
$\frac{t_{\Phi PIH}}{t_{\Phi PIL}}$	ΦP Clock Input High/Low Ratio		0.9	1.0	1.1	–
$t_{\Phi PIHL}$	ΦP Clock Input High to Low Transition Time		–	–	$\frac{0.15}{f_{\Phi P}}$	–
V_{REIL}	$\overline{\text{Reset}}$ Input Low Voltage	35	–	–	1.2	V
V_{REIH}	$\overline{\text{Reset}}$ Input High Voltage		2.4	–	–	V
t_{REIL}	$\overline{\text{Reset}}$ Input Low Time		2	–	–	µs
V_{LCIL}	Luma/Chroma Input Low Voltage	57 to 66	–	–	0.4	V
$-I_{LCIH}$	Luma/Chroma Input High Current		–	–	20	µA
$t_{\Phi PLCIH}$	Luma/Chroma Input Hold Time after ΦP Clock Input	57 to 66, 68	13	–	–	ns
$t_{LCIS\Phi P}$	Luma/Chroma Input Setup Time before ΦP Clock Input		17	–	–	ns
V_{DIL}	RAM Data Input Low Voltage	10 to 17	–	–	0.8	V
V_{DIH}	RAM Data Input High Voltage		2.0	–	–	V
$t_{\Phi PDIH}$	RAM Data Input Hold Time after ΦP Clock Input	10 to 17, 68	15	–	–	ns
$t_{DIS\Phi P}$	RAM Data Input Setup Time before ΦP Clock Input		0	–	–	–
V_{FSIL}	Fast Switching Input Low Voltage	23	–	–	0.4	V
V_{FSIH}	Fast Switching Input High Voltage		0.7	–	–	V
V_{RGBIL}	RGB Analog Input Low Voltage	24 to 26	0	–	–	V
V_{RGBIH}	RGB Analog Input High Voltage		–	–	V_{SUP}	–
V_{MSKIL}	Skew Data (Main) Input Low Voltage	44	–	–	0.4	V
$-I_{MSKIH}$	Skew Data (Main) Input High Current		–	–	20	µA

Recommended Operating Connections, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
$t_{\Phi MSKIH}$	Skew Data (Main) Input Setup Time before ΦM Clock Input	44, 50	13	–	–	ns
$t_{MSKIS\Phi}$	Skew Data (Main) Input Setup Time before ΦM Clock Input		17	–	–	ns
V_{MHBIL}	Delayed Horizontal Blanking Pulse (Main) Input Low Voltage	45	–	–	3.2	V
V_{MHBIH}	Delayed Horizontal Blanking Pulse (Main) Input High Voltage		3.6	–	–	V
V_{MVBIL}	Delayed Horizontal Blanking Pulse (Main) Input Low Voltage		–	–	0.8	V
V_{MVBIL}	Delayed Horizontal Blanking Pulse (Main) Input High Voltage		2.4	–	–	V
$t_{\Phi MHVBIH}$	Del. Hor. and Vert. Blanking Pulse (Main) Input Hold Time after ΦM Clock Input	45, 50	13	–	–	ns
$t_{MHVBIS\Phi}$	Del. Hor. and Vert. Blanking Pulse (Main) Input Setup Time before ΦM Clock Input		17	–	–	ns
V_{PHBIL}	Delayed Horizontal Blanking Pulse (PIP) Input Low Voltage	55	–	–	3.2	V
V_{PHBIH}	Delayed Horizontal Blanking Pulse (PIP) Input High Voltage		3.6	–	–	V
V_{PVHBIL}	Vertical Blanking Pulse (PIP) Input Low Voltage		–	–	0.8	V
V_{PVBIH}	Vertical Blanking Pulse (PIP) Input High Voltage		2.4	–	–	V
$t_{\Phi PHVBIH}$	Del. Hor. and Vert. Blanking Pulse (PIP) Input Hold Time after ΦP Clock Input	55, 68	13	–	–	ns
$t_{PHVBIS\Phi}$	Del. Hor. and Vert. Blanking Pulse (PIP) Input Setup Time before ΦP Clock Input		17	–	–	ns
V_{PSKIL}	Skew Data (PIP) Input Low Voltage	56	–	–	0.4	V
$-I_{PSKIH}$	Skew Data (PIP) Input High Current		–	–	20	µA
$t_{\Phi PSKIH}$	Skew Data (PIP) Input Hold Time after ΦP Clock Input	56, 68	13	–	–	ns
$t_{PSKIS\Phi}$	Skew Data (PIP) Input Setup Time before ΦP Clock Input		17	–	–	ns

Recommended Operating Connections, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{MSIL}	Msync Input Low Voltage	31	–	–	0.4	V
$-I_{MSIH}$	Msync Input High Current		–	–	20	µA
$t_{\Phi MSIH}$	Msync Input Hold Time after ΦM Clock Input	31, 50	13	–	–	ns
$t_{MSIS\Phi}$	Msync Input Setup Time before ΦM Clock Input		17	–	–	ns
V_{IMIL}	IM Bus Input Low Voltage	52 to 54	–	–	0.8	V
V_{IMIH}	IM Bus Input High Voltage		2.4	–	–	V
$f_{\Phi I}$	ΦI IM Bus Clock Frequency		0.05	–	170	kHz
t_{IM1}	ΦI Clock Input Delay Time after IM Bus Ident Input		0	–	–	–
t_{IM2}	ΦI Clock Input Low Pulse Time		3.0	–	–	µs
t_{IM3}	ΦI Clock Input High Pulse Time		3.0	–	–	µs
t_{IM4}	ΦI Clock Input Setup Time before Ident Input High		0	–	–	–
t_{IM5}	ΦI Clock Input Hold Time after Ident Input High		1.5	–	–	µs
t_{IM6}	ΦI Clock Input Setup Time before End–Pulse Input		6.0	–	–	µs
t_{IM7}	IM Bus Data Input Delay Time after ΦI Clock Input		0	–	–	–
t_{IM8}	IM Bus Data Input Setup Time before ΦI Clock Input		0	–	–	–
t_{IM9}	IM Bus Data Input Hold Time after ΦI Clock Input		0	–	–	–
t_{IM10}	IM Bus Ident End–Pulse Low Time		3.0	–	–	µs

2.5.3. Characteristics at T_A = 0 to 65 °C, V_{SUP} = 4.75 to 5.25 V, $f_{\Phi M}$ = 14.3 to 20.25 MHz, $f_{\Phi P}$ = 14.3 to 20.25 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SUP}	Supply Current	18+49+67	–	150	180	mA	
I_{LCOH}	Luma/Chroma Output High Current	31 to 34, 36 to 43	–	–	10	µA	V_{LCO} = 5 V
V_{LCOL}	Luma/Chroma Output Low Voltage		–	–	0.3	V	I_{LCO} = 4.5 mA or Pull–up Resistor 1 kΩ, C_L = 20 to 60 pF
t_{LCOHL}	Luma/Chroma Output High to Low Transition Time		–	–	10	ns	
t_{LCOPD}	Luma/Chroma Output Propagation Delay Time	31 to 34, 36 to 43	–	25	–	ns	
t_{LCOH}	Luma/Chroma Output Hold Time		–	10	–	ns	
$-I_{LCIL}$	Luma/Chroma Input Low Current	57 to 66	–	1.0	2.0	mA	V_{LCI} = 0.3 V
V_{LCIH}	Luma/Chroma Input High Voltage		–	–	1.2	V	I_{LCI} = 0
t_{LCIS}	Luma/Chroma Input Setup Time		–	10	–	ns	
t_{LCIH}	Luma/Chroma Input Hold Time		–	5	–	ns	
C_{LCI}	Luma/Chroma Input Capacitance		–	3.0	–	pF	I_{LCI} = 0
$-I_{FSIL}$	Fast Switching Input Low Current	23	–	1.0	2.0	mA	V_{FSI} = 0.3 V
V_{FSIH}	Fast Switching Input High Voltage		–	–	1.2	V	I_{FSI} = 0
C_{FSI}	Fast Switching Input Capacitance		–	3.0	–	pF	I_{FSI} = 0
$-I_{SKIL}$	Skew Data Input Low Current	44, 56	–	1.0	2.0	mA	V_{SKI} = 0.3 V
V_{SKIH}	Skew Data Input High Voltage		–	–	1.2	V	I_{SKI} = 0
C_{SKI}	Skew Data Input Capacitance		–	3.0	–	pF	I_{SKI} = 0
V_{AOL}	RAM Address Output Low Voltage	2 to 9, 68	–	–	0.4	V	I_{AO} = 3.2 mA
V_{AOH}	RAM Address Output High Voltage		2.4	–	–	V	$-I_{AO}$ = 0.8 mA
$t_{DAO\Phi P}$	RAM Address Output Delay Time after ΦP Clock Input	2 to 9, 68	0	–	25	ns	I_{AO} = 3.2 mA, $-I_{AO}$ = 0.8 mA, C_L = 100 pF max.
V_{CASOL}	$\overline{CAS}$ Output Low Voltage	20	–	–	0.4	V	I_{CASO} = 3.2 mA
V_{CASOH}	$\overline{CAS}$ Output High Voltage		2.4	–	–	V	$-I_{CASO}$ = 0.8 mA
$t_{DCAS\Phi P}$	$\overline{CAS}$ Output Delay Time after ΦP Clock Input	20, 68	0	–	20	ns	I_{CASO} = 3.2 mA, $-I_{CASO}$ = 0.8 mA, C_L = 100 pF max.
V_{RASOL}	$\overline{RAS}$ Output Low Voltage	21	–	–	0.4	V	I_{RASO} = 3.2 mA
V_{RASOH}	$\overline{RAS}$ Output High Voltage		2.4	–	–	V	$-I_{RASO}$ = 0.8 mA
$t_{DRAS\Phi P}$	$\overline{RAS}$ Output Delay Time after ΦP Clock Input	21, 68	0	–	25	ns	I_{RASO} = 3.2 mA, $-I_{RASO}$ = 0.8 mA, C_L = 100 pF max.
V_{WEOL}	$\overline{WE}$ Output Low Voltage	22	–	–	0.4	V	I_{WEO} = 3.2 mA
V_{WEOH}	$\overline{WE}$ Output High Voltage		2.4	–	–	V	$-I_{WEO}$ = 0.8 mA

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
$t_{DWE\Phi P}$	$\overline{WE}$ Output Delay TIme after ΦP Clock Input	22, 68	0	–	25	ns	I_{WEO} = 3.2 mA, $-I_{WEO}$ = 0.8 mA C_L = 100 pF max.
V_{FSOL}	Fast Switching Output Low Voltage	30	–	–	0.4	V	I_{FSO} = 3.2 mA
V_{FSOH}	Fast Switching Output High Voltage		2.4	–	–	V	$-I_{FSO}$ = 0.8 mA
$t_{DFSO\Phi M}$	Fast Switching Output Delay Time after ΦM Clock Input for Analog Border	22, 50	0+ skew/16 ΦM where skew = 0 to 15	–	30+ skew/16 ΦM	–	I_{FSO} = 3.2 mA $-I_{FSO}$ = 0.8 mA C_L = 20 to 60 pF
V_{ODOL}	VPU Outputs Disable Output Low Voltage	47	–	–	0.4	V	I_{ODO} = 3.2 mA
V_{ODOH}	VPU Outputs Disable Output High Voltage		2.4	–	–	V	$-I_{ODO}$ = 0.8 mA
V_{ODOHI}	VPU Outputs Disable Output High Impedance Voltage		–10	–	+10	µA	V_{ODO} = 0 to +5 V
$t_{DODO\Phi M}$	VPU Outputs Disable Output Delay Time after ΦM Clock Input for Digital Insertion Mode	47, 50	0	–	30	ns	I_{ODO} = 3.2 mA, $-I_{ODO}$ = 0.8 mA, C_L = 20 to 60 pF
$t_{DODO\Phi M}$	VPU Outputs Disable Output Delay Time after ΦM Clock Input for Stand–Alone Mode		0+ skew/16 ΦM where skew = 0 to 15	–	30+ skew/16 ΦM	–	I_{ODO} = 3.2 mA, $-I_{ODO}$ = 0.8 mA, C_L = 20 to 60 pF
V_{IMPL}	IM Bus Port Output Low Voltage	46	–	–	0.4	V	I_{IMP} = 3.2 mA
V_{IMPH}	IM Bus Port Output High Voltage		2.4	–	–	V	$-I_{IMP}$ = 0.8 mA
V_{RGBAN}	RGB Analog Output Analog Voltage	27 to 29	equal to the input voltage at pins 24 to 26, BW = 0 to 4 MHz				
V_{RGBBL}	RGB Analog Output Border Low Voltage		–	–	0.4	V	I_{RGBB} = 0.44 mA
V_{RGBBH}	RGB Analog Output Border High Voltage		4.6	–	–	V	$-I_{RGBB}$ = 0.16 mA
V_{DOL}	RAM Data Output Low Voltage	10 to 17	–	–	0.4	V	I_{DO} = 3.2 mA
V_{DOH}	RAM Data Output High Voltage		2.4	–	–	V	$-I_{DO}$ = 0.8 mA
I_{DOHI}	RAM Data Output High Impedance Output Current		–10	–	+10	µA	V_{DO} = 0 to +5 V
V_{IMOL}	IM Bus Data Output Low Voltage	54	–	–	0.4	V	I_{IMO} = 3 mA
V_{IMOH}	IM Bus Data Output High Current		–	–	10	µA	V_{IMO} = 5 V

2.5.4. Input/Output Timing

Input setup times, input hold times, and output delays are always referenced to the trailing edge of clock ΦM or ΦP respectively, unless otherwise specified (Fig. NO TAG). Abbreviated pin names are used in timing descriptions.

Input YUV bus (L2 to L7 luma inputs and C0 to C3 chroma inputs, pins 57 to 66) and deflection/timing signals (PHVBIN and PSKEW, pins 55 and 56) of the small picture to be inserted are referenced to the trailing edge of the ΦP PIP clock (pin 68).

All DRAM interface signals – address, Data input/output, and control (RAS and WE) – are referenced to the trailing edge of the ΦP PIP clock except for the CAS signal, which is referenced to the leading edge of ΦP.

Output YUV bus (L0 to L7 luma outputs and C0 to C3 chroma outputs, pins 31 to 34 and 36 to 43) and deflection/timing signals (MHVBIN, MSKEW and ODOUT, pins 44, 45 and 47) of the output picture processing are referenced to the trailing edge of the ΦM main clock.

FSIN fast switching input (pin 23) and Reset (pin 35) may be asynchronous to either clock. FSOUT fast switching output, when representing analog border timing (with FSIN = logic 1, is referenced to the trailing edge of ΦM main clock.

RGB outputs (pins 27 to 29) will follow analog RGB inputs (pins 24 to 26) with DC to 4 MHz bandwidth when FSIN = logic 0. They will represent DC digital values of analog border when FSIN = logic 1.

The IM bus signals Ident and Data are referenced to the IM bus clock (Fig. 2–14). The IM bus is explained in section 4.

2.5.5. Waveforms

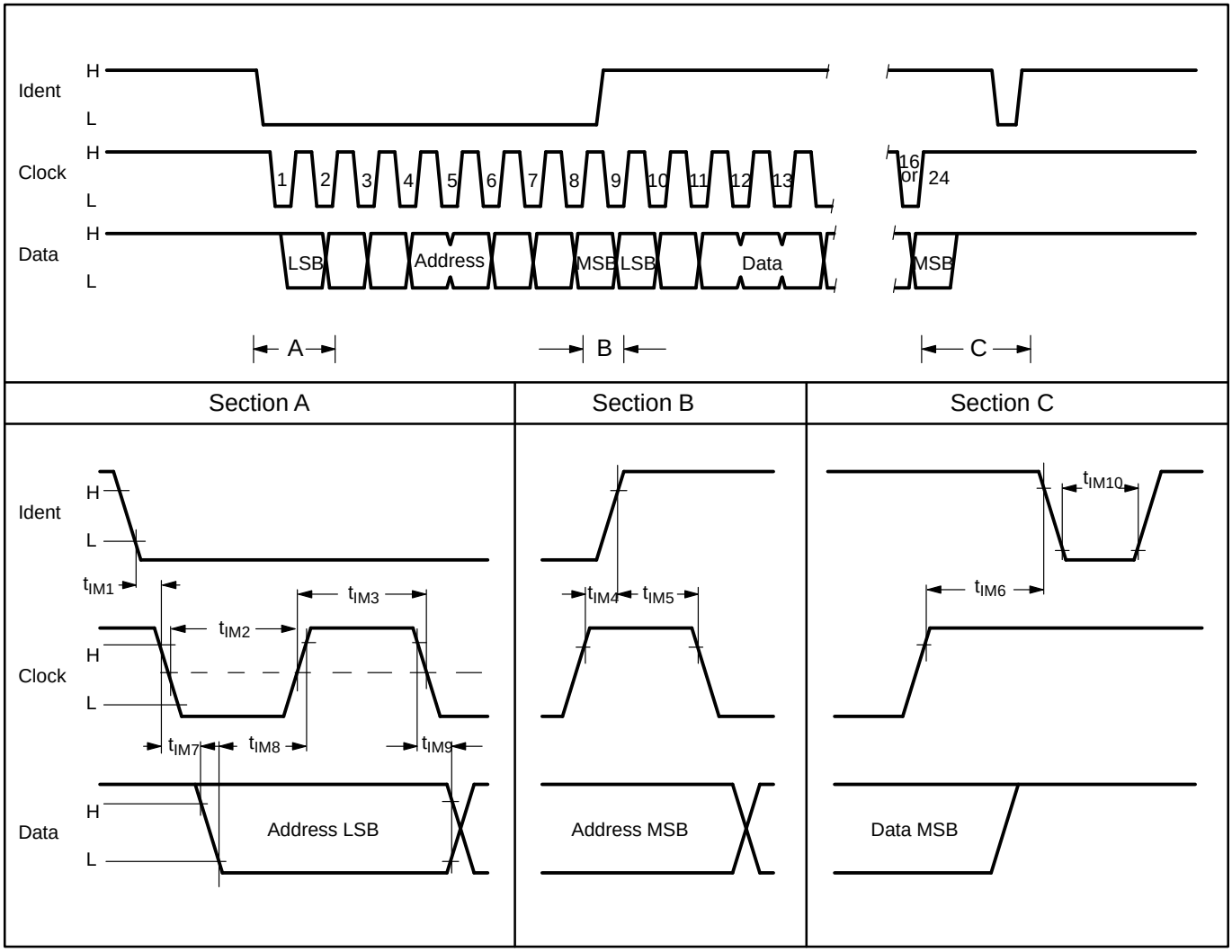

Fig. 2–14: IM bus waveforms

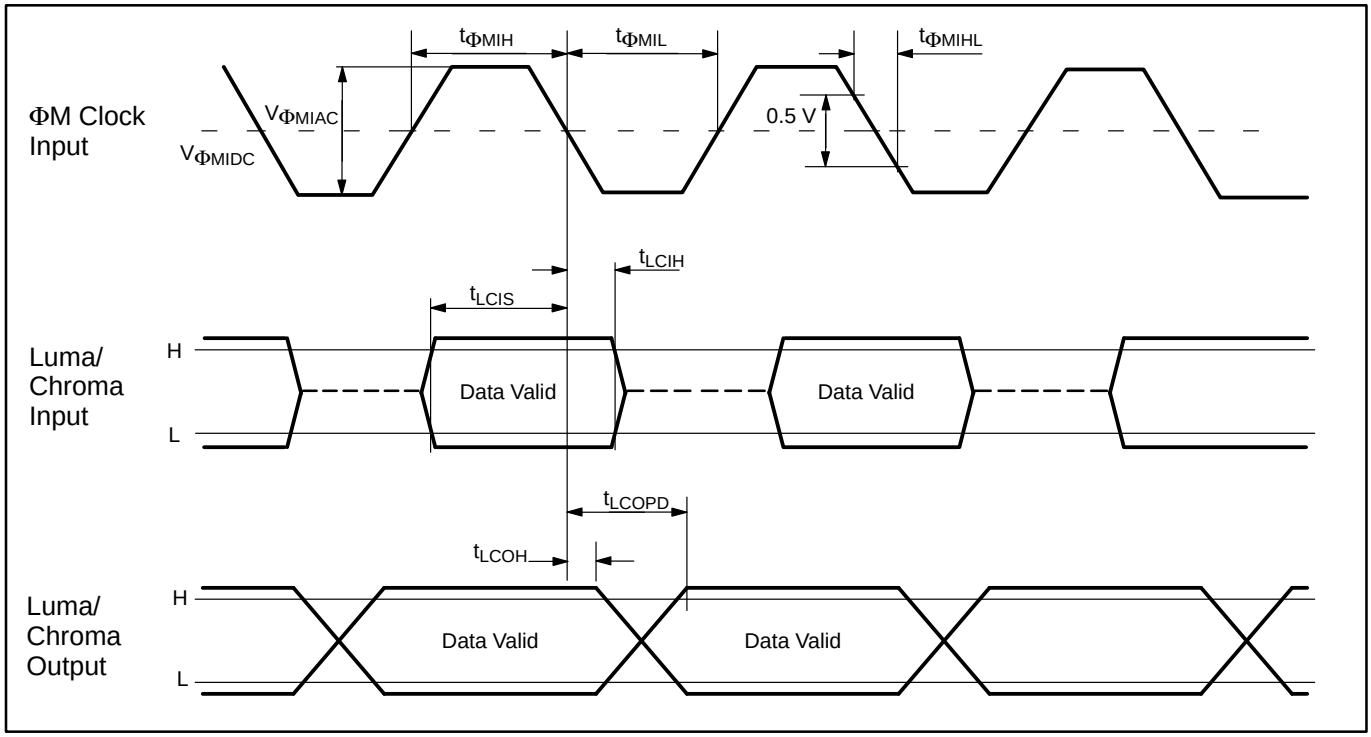

Fig. 2–15: Digital clock, luma and chroma waveforms

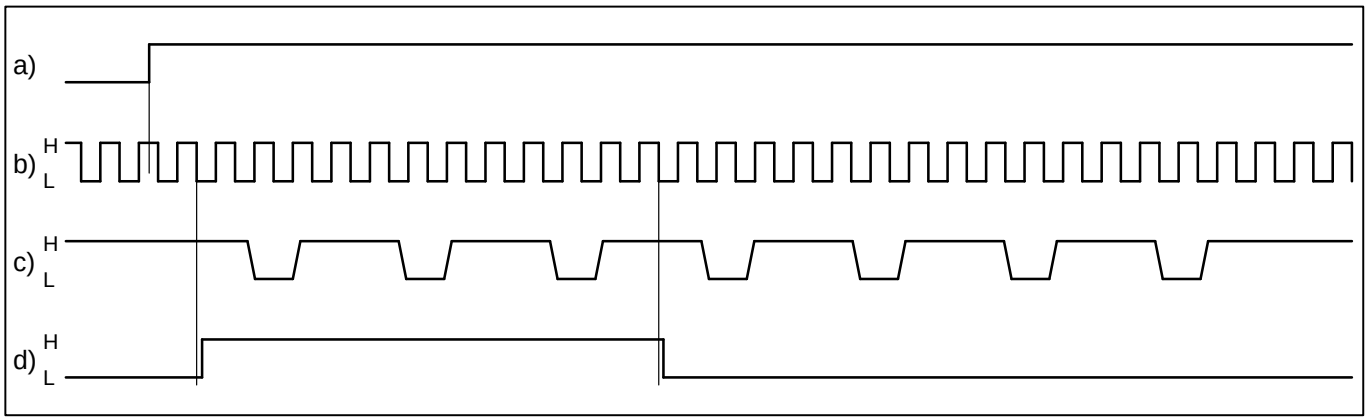

Fig. 2–16: D2–MAC/SECAM chroma sync scheme
a) undelayed horizontal blanking
b) ΦM main clock
c) chroma output C0
d) window opened in VCU after horizontal blanking

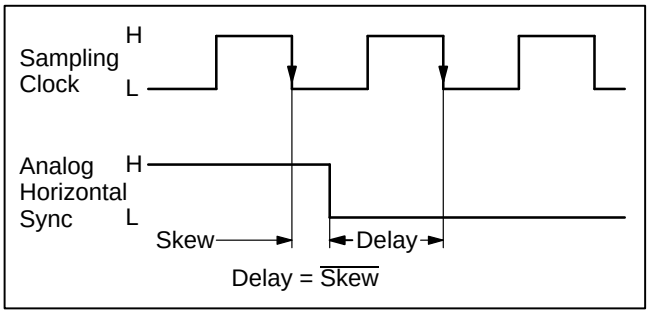

Fig. 2–17: Definition of skew

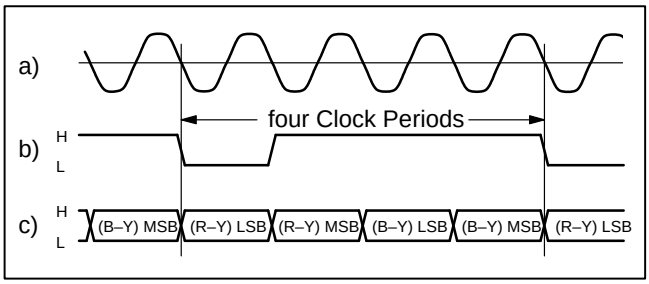

Fig. 2–18: Close up of NTSC/PAL chroma sync scheme
a) ΦM main clock
b) chroma bus bit 0 as sync pulse during sync window
c) time multiplexed chroma bus, with sync pulse coincident to (R–Y) LSB

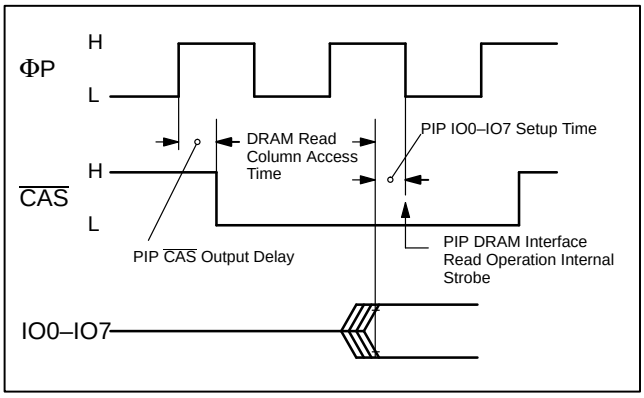

Fig. 2–19: Close up of DRAM page mode read timing

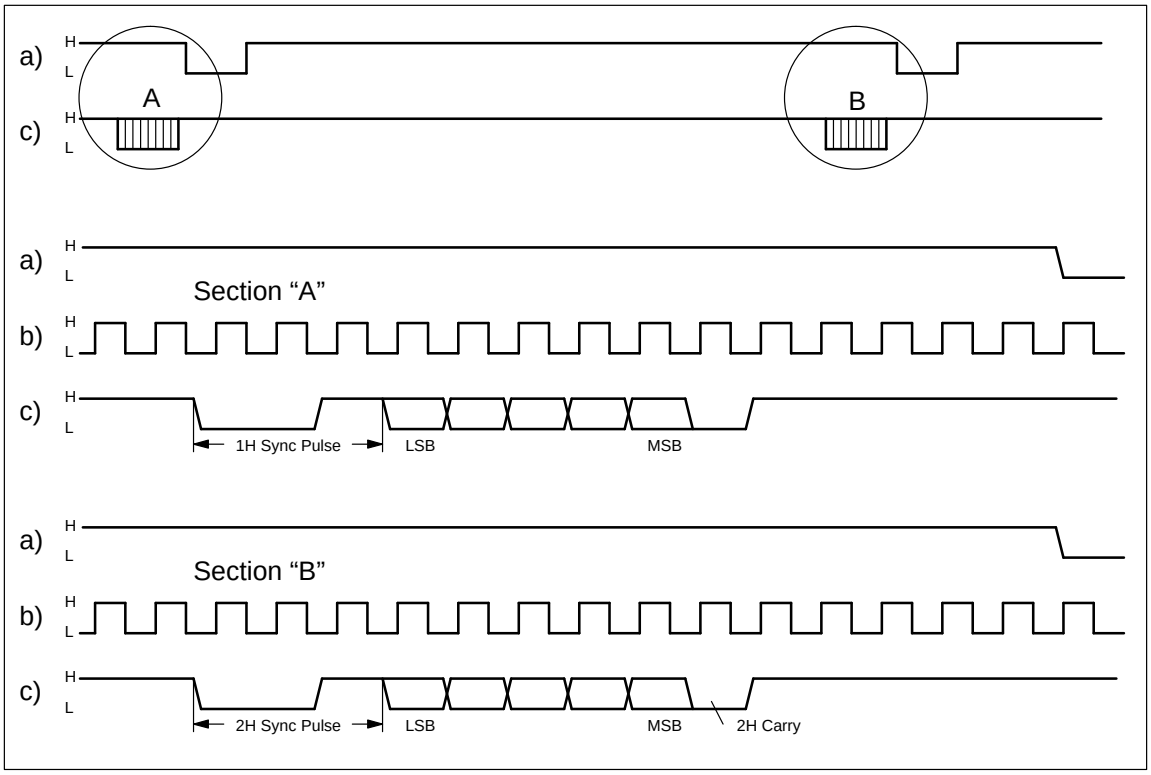

Fig. 2–20: Skew data format
a) delayed horizontal blanking
b) ΦM system clock
c) skew data

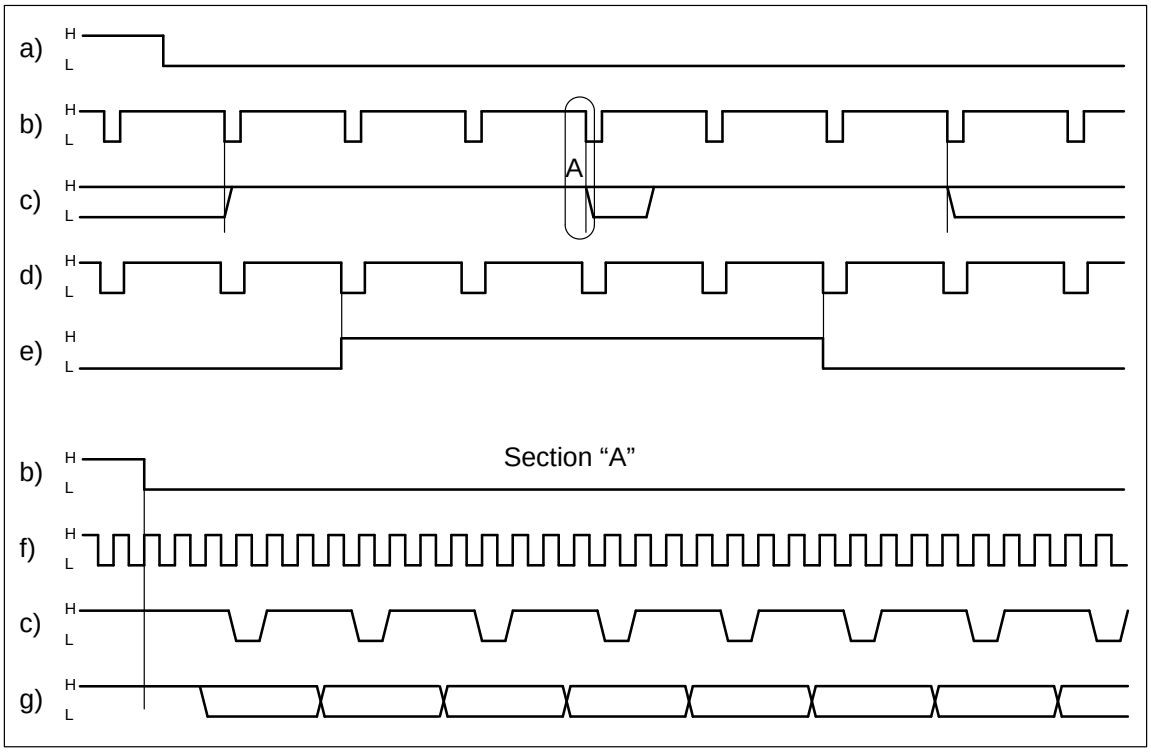

Fig. 2–21: NTSC/PAL chroma sync scheme
a) vertical blanking
b) color key pulse
c) chroma output C0
d) undelayed horizontal blanking
e) window opened in VCU during vertical blanking
f) ΦM system clock
g) chroma output C3

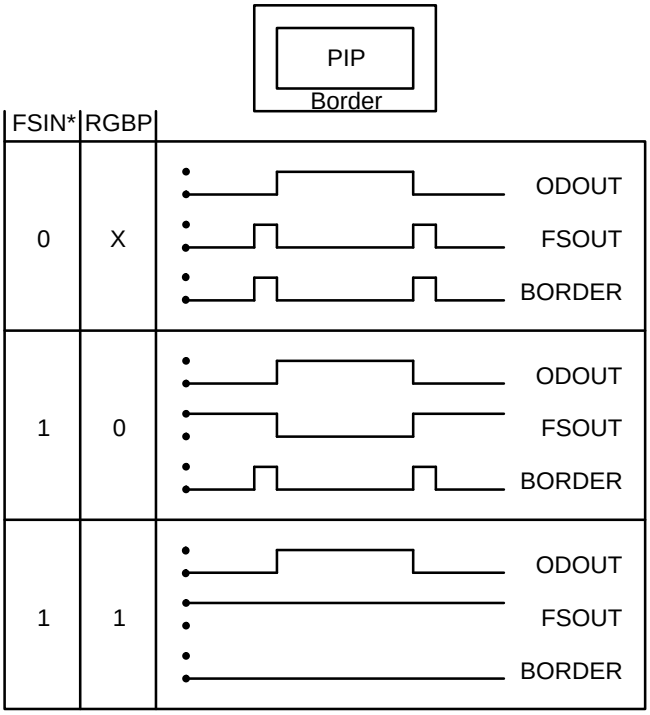

Fig. 2–22: FSOUT fast switching and ODOUT outputs disable output waveforms for STA = 0 and BDI = 0

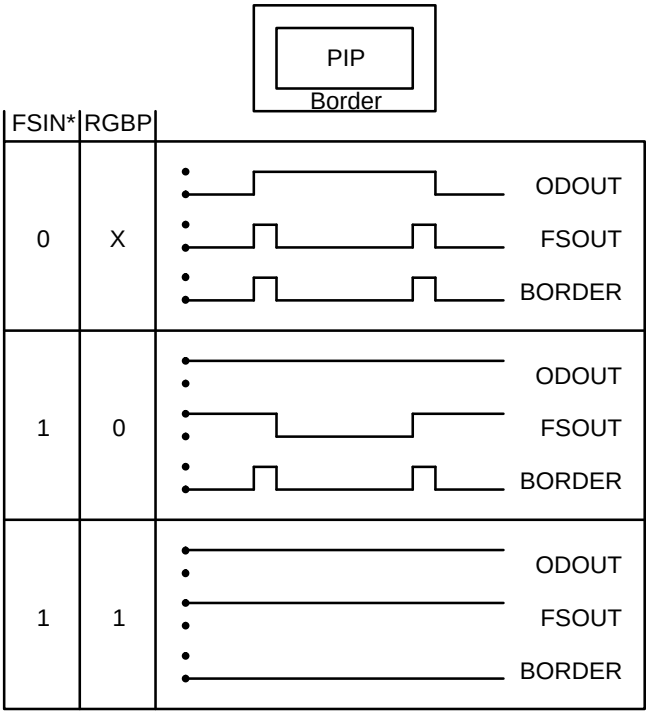

Fig. 2–24: FSOUT fast switching and ODOUT outputs disable output waveforms for STA = 1 and BDI = 0

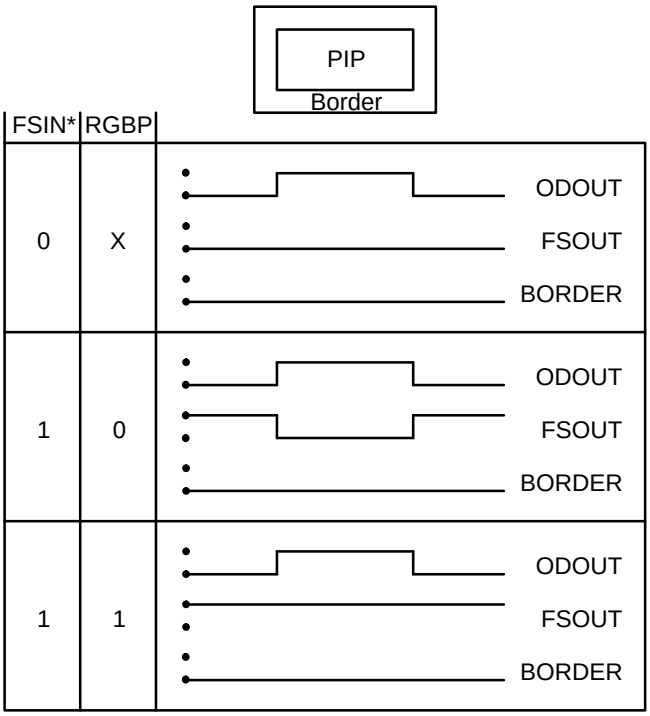

Fig. 2–23: FSOUT fast switching and ODOUT outputs disable output waveforms for STA = 0 and BDI = 1

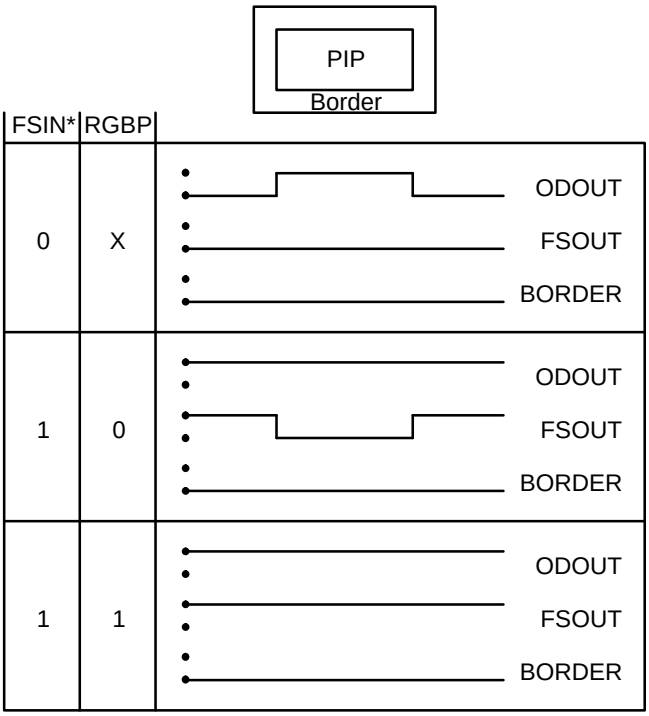

Fig. 2–25: FSOUT fast switching and ODOUT outputs disable output waveforms for STA = 1 and BDI = 1

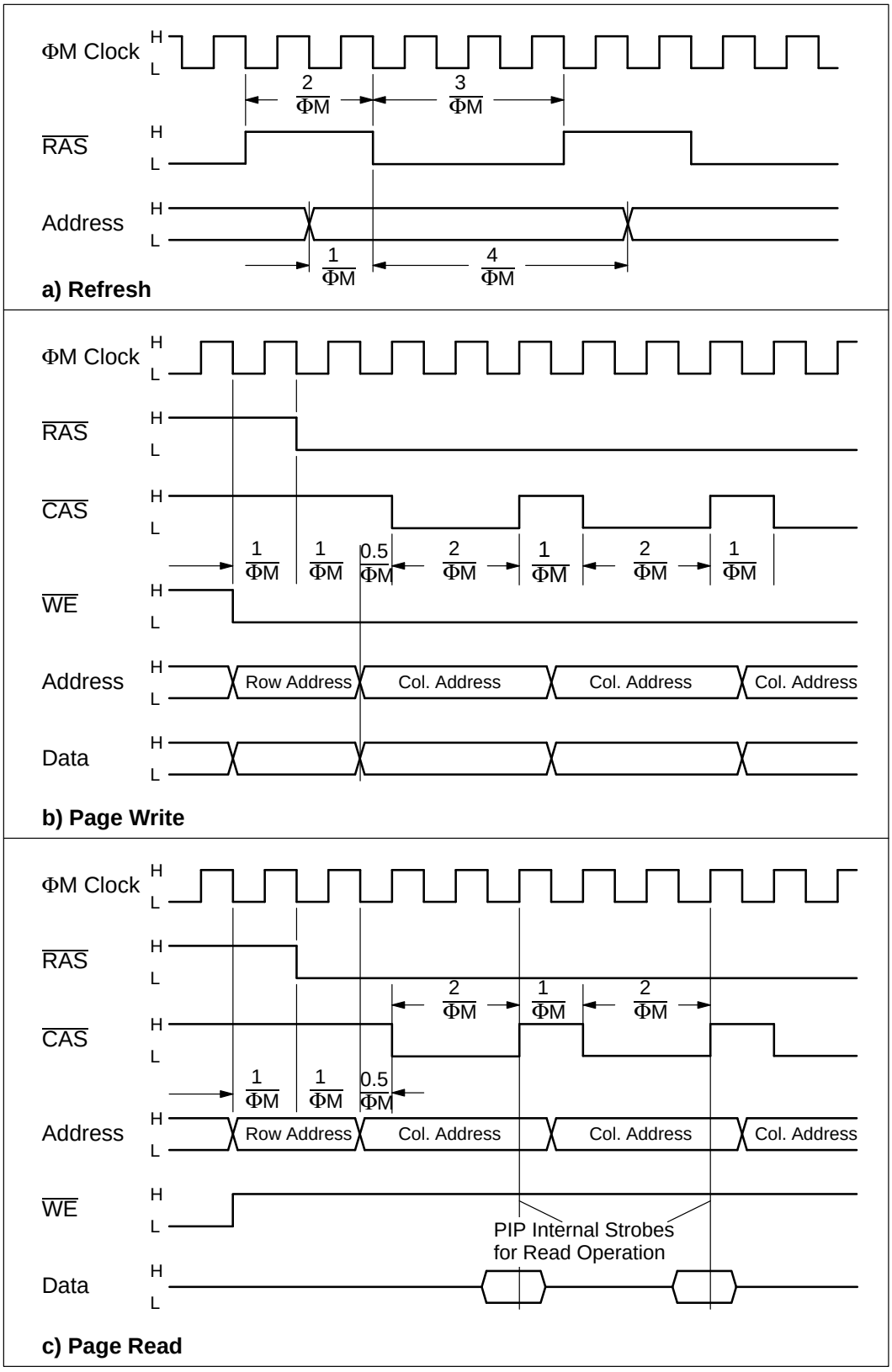

Fig. 2–26: DRAM interface timing
a) refresh mode
b) page write mode
c) page read mode

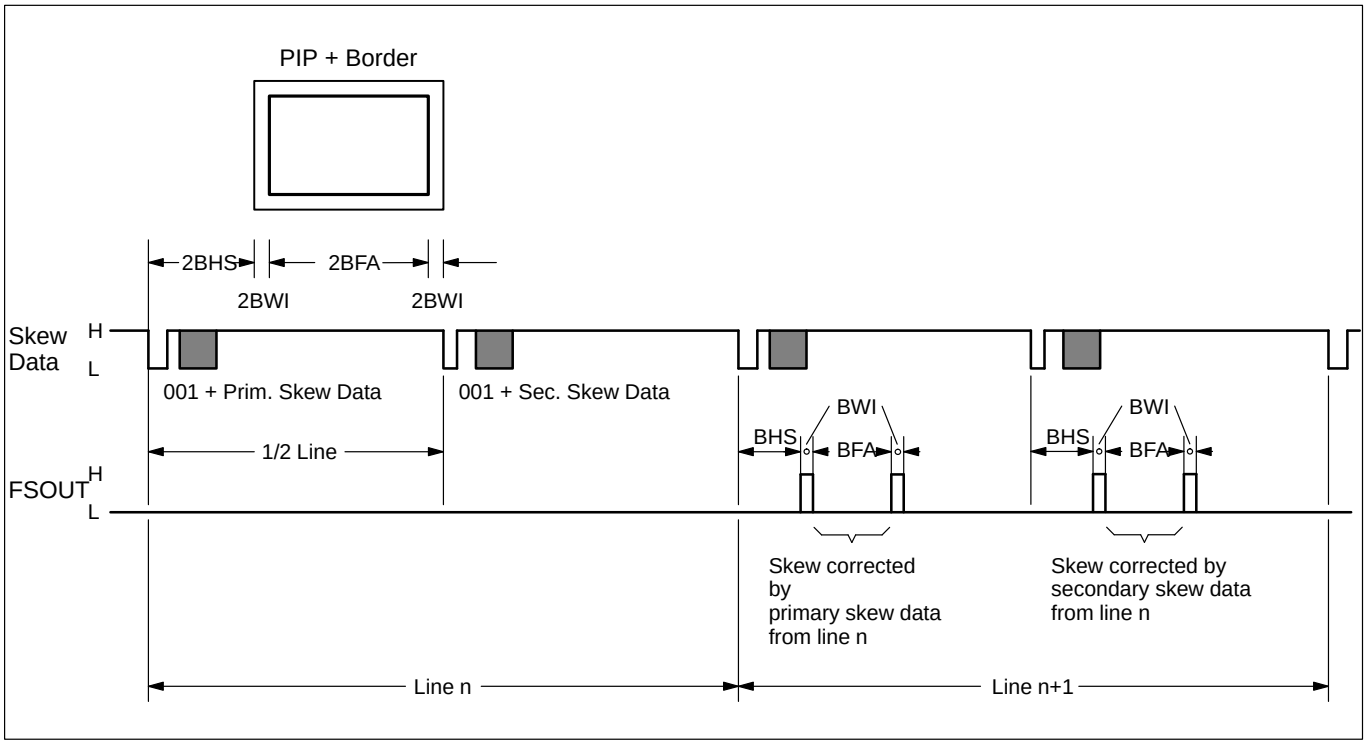

Fig. 2–27: 2H proscan mode FSOUT waveform

3. Functional Description

As can be seen from Fig. 1–1, the PIP 2250 Picture–in–Picture Processor is made up of four major functional blocks; input picture processing, output picture processing, DRAM interface and IM bus interface. For better understanding, two features used in digital TV receivers according to the DIGIT 2000 concept may be described first: skew data and chroma timing synchronization.

3.1. Skew Data

The skew data signal produced by the DPU 2553 or similar deflection processor or the VSP 2860 Video Sync Processor is used to align the phase position of the video signal in the PIP 2250, as shown in Fig. 2–20. The skew data input is normally High, or at logic 1, when inactive. At the horizontal start (start of each line), it becomes active (Low) with a header code of 001 or 011 followed by 5 bits of luma skew data (or 6 bits if 2H carry is included). Thus the start of header code is defined as any 0 preceded by 9 or more 1s.

Luma skew is defined as the phase or time difference between the sampling clock and the analog horizontal sync expressed in resolution of 1/32 of the sampling clock period (Fig. 2–17). This phase difference changes from line to line because the sampling clock frequency may not be a multiple of the analog horizontal frequency. As a result, digital samples on one line may not align vertically with those from the adjacent lines. For signal processing in the vertical direction, like in PIP input picture processing, samples on each line must be interpolated by the amount of skew so that corresponding samples on different lines are aligned vertically.

Thus the skew data defines the horizontal start timing and carries information about the amount of luma skew. Notice the horizontal start is **NOT** derived from the horizontal blanking.

3.2. Chroma Timing Synchronization

The 4–bit chroma transfer on the YUV bus is time multiplexed for R–Y and B–Y. There must be some scheme to synchronize the timing. There are two schemes for chroma timing synchronization: either for PAL and NTSC, or for D2–MAC and SECAM.

For the PAL/NTSC scheme, bit 0 of chroma bus no longer carries video information, but is used as a sync signal for chroma timing synchronization during vertical blanking. Using horizontal blanking as the basis for line count, at the 4th line after vertical blanking trailing edge, chroma bus bit 0 will be a string of 72 (negative pulses with 25 % duty cycle (Fig. 2–21). The negative pulses are synchronized to the R–Y LSB timing of chroma bus (Fig. 2–18). In addition, it doubles as the clock for the transmission of 72 bits of data for VCU control with data from bit 3 of the chroma bus.

For the D2–MAC/SECAM scheme, chroma synchronization occurs every horizontal line, again with chroma bus bit 0 being a string of three 25 % cycle negative pulses synchronized to the R–Y LSB chroma bus timing (Fig. 2–16). The sync pulses start after the leading edge of horizontal blanking and last for 12 clocks.

3.3. Input Picture Processing

The input picture processing block (Fig. 3–2) defines a window for the input picture to be processed. Parameters IHS, IVS and IVSI (Fig. 3–1) define the location and size of this window. Samples within the window are reduced by a factor of 1/3 in both horizontal and vertical direction, for a reduction to 1/9 of the original picture size.

Input to the input picture processing is a digitized picture in the form of an input YUV bus and timing/deflection signals, as are skew data, horizontal blanking and vertical blanking. They may come from the VSP 2860 Video/ Sync Processor or a similar source.

Because of the reduction in picture size described above, internally only 5 bits resolution is needed for luma (Y) and 6 bits for chroma (UV). This results in only 5 pins for luma at the input YUV bus. However, four pins are still needed for the multiplexed chroma bus even though only 6 bits after demultiplexing are needed.

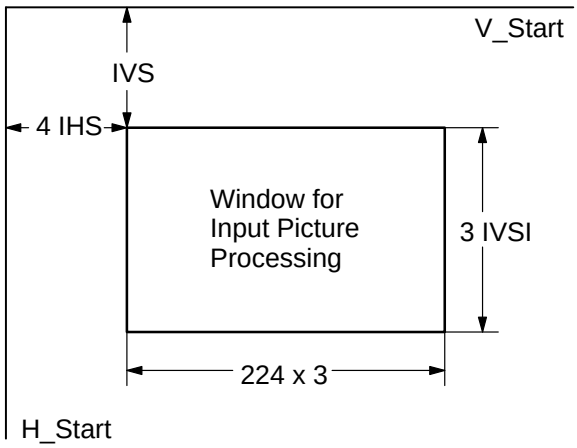

Fig. 3–1: Input picture processing parameters

3.3.1. Input Luma Processing

This section includes skew correction, peaking control, and lowpass filtering followed by vertical filtering at a rate of four times the color subcarrier frequency, i.e. the ΦP clock frequency (see Fig. 3–1). The number of samples processed per line is 224 x 3. Skew correction takes the form of

$H(z) = (Delay/4)z^{-1} + (1 - Delay/4)$

where Delay = luma delay = inverse of luma skew data.

Two bits from register 42 control four selections for peaking parameters P with the following characteristics:

$$H(z) = z^{-6} + PEA/8 \cdot (z^{-6} - 1) \cdot (1 - z^{-6})$$

where PEA can be 1, 2, 4 or 8. After peaking, luma may become a signed (negative) number.

Lowpass filtering performs the function of anti–aliasing for decimation. It has the following characteristic:

$$H(z) = (1 + z^{-2}) \cdot (1 + z^{-2}) \cdot (1 + z^{-1})/8$$

followed by a limiter which converts the luma back to a 5–bit unsigned number within the range of (0, 31). The last step in luma processing is vertical filtering of averaging three lines with:

$$H(z) = (1 - K) \cdot H^{-1} + K$$

where K = 1, a/2 and 1/4 for the first, second and third lines respectively, and H–1 is the average from one line earlier. The luma line buffers store the intermediate (first or second lines) or final (third lines) results (IPDATA3 – IPDATA7) after vertical filtering. The number of 5–bit luma samples stored in the line buffer is 224.

3.3.2. Input Chroma Processing

This section includes lowpass filtering, skew correction followed by vertical filtering, all time–shared for R–Y and B–Y chroma components at a rate of two times the color subcarrier. The number of samples processed per line is 56 x 3 for each component. After demultiplexing, 6 bits of chroma pass through the lowpass filter section for anti–aliasing of decimation with the following characteristics:

$$H(z) = (1 + z^{-4}) \cdot (1 + z^{-6})$$

Skew correction is done according to:

$$H(z) = \frac{(Delay/4)\ \ z^{-2} + (1 - Delay/4)}{4}$$

where Delay = chroma delay is determined by chroma bus timing.

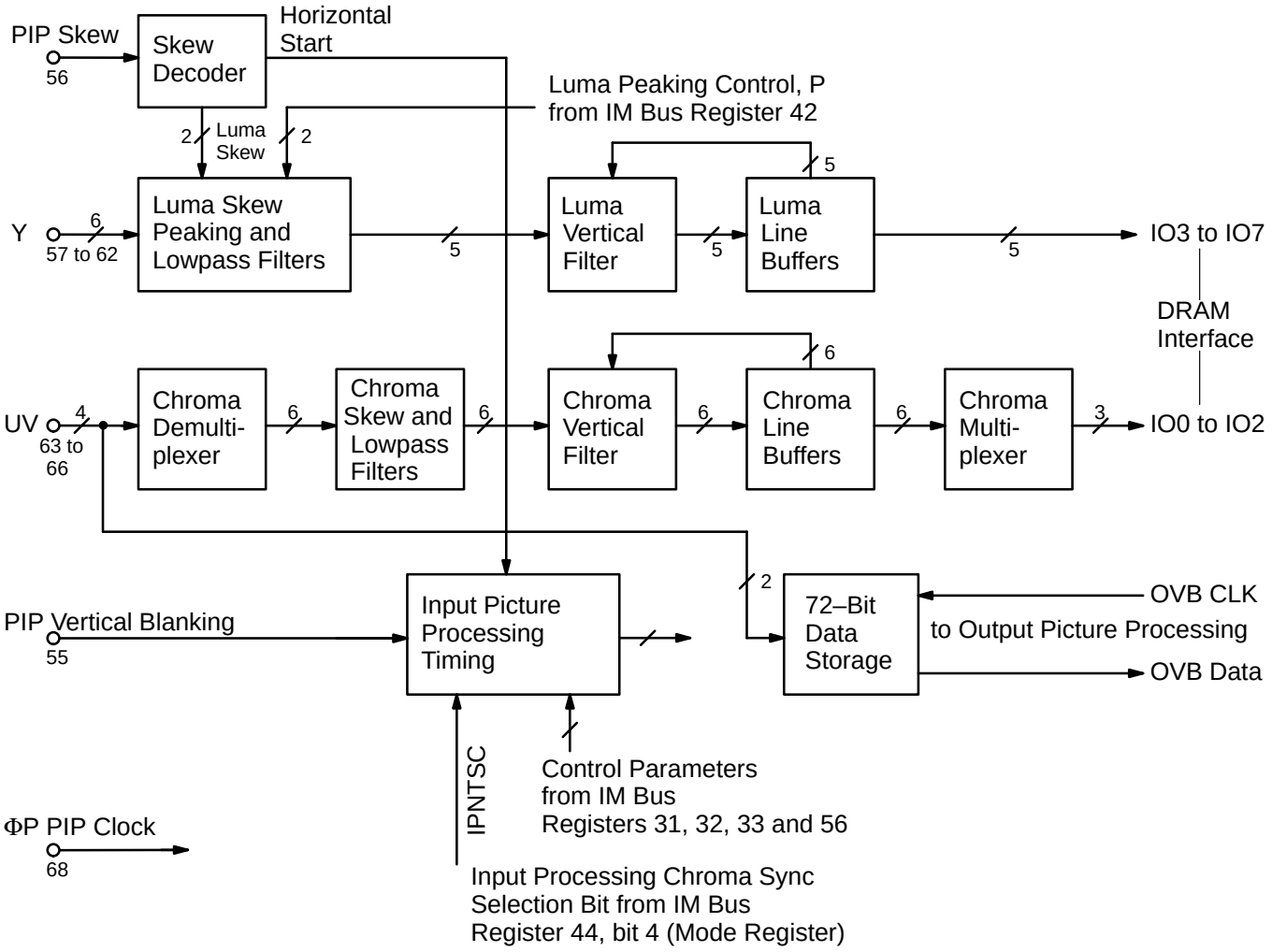

Fig. 3–2: Input picture processing block diagram

Edition: March 3, 1992
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Vertical filtering is done the same way as in the luma processing. However, the 6–bit chroma R–Y and B–Y outputs from chroma line buffer is multiplexed to 3 bits (IPDATA0 – IPDATA2) in the sequence of (R–Y)LSB, (R–Y)MSB (B–Y)LSB, (B–Y)MSB for DRAM interface. The number of multiplexed 3–bit chroma samples from the chroma line buffer is the 56 x 2 x 2 = 224. So, during input picture processing, 224 samples of 5–bit luma (IPDATA3 – IPDATA7) and 3–bit chroma (IPDATA0 – IPDATA2), or 224 Bytes, are generated every 3 lines (or 64 ms x 3 = 192 ms), for possible storage into the external DRAMs.

3.3.3. Parameters for Control of Input Picture Processing

As mentioned earlier, parameters IHS, IVS and IVSI control the location and size of the picture processing window. They are programmable via registers 31, 32 and 33 respectively. In addition, since luma and chroma have different sampling rates, they have different delays after input picture processing. To equalize the delays, parameter LD which is programmable through register 56, adds delay to the luma processing path.

For input picture chroma synchronization, bit 4 of register 44 determines the scheme used for this purpose.

For external DRAM interface, although 224 Bytes of data is generated every three lines, not all 224 Bytes may be stored. IBY defines the number of Bytes to be transferred per line of reduced picture. IRA and ICA define starting row and column addresses of the DRAMs for data storage. For more details see section 4.

3.3.4. 72–Bit Data for VCU Control

For VCU control, 72 bits of data may be transmitted during vertical blanking via bits 0 and 3 of chroma bus as serial clock and data, as described in section 3.2. These 72 bits of data are stored in the 72–bit data storage block. They are retrieved and sent out onto the output chroma bus during the main picture vertical blanking if PIP is used in a stand–alone application (section 3.4.1.1.).

3.4. Output Picture Processing

This section retrieves the data representing the reduced picture from the line buffers one line at a time and sends them out to the YUV bus to be merged with the main picture for a picture–in–picture effect. In addition, a border is added to the small picture (see Fig. 3–3).

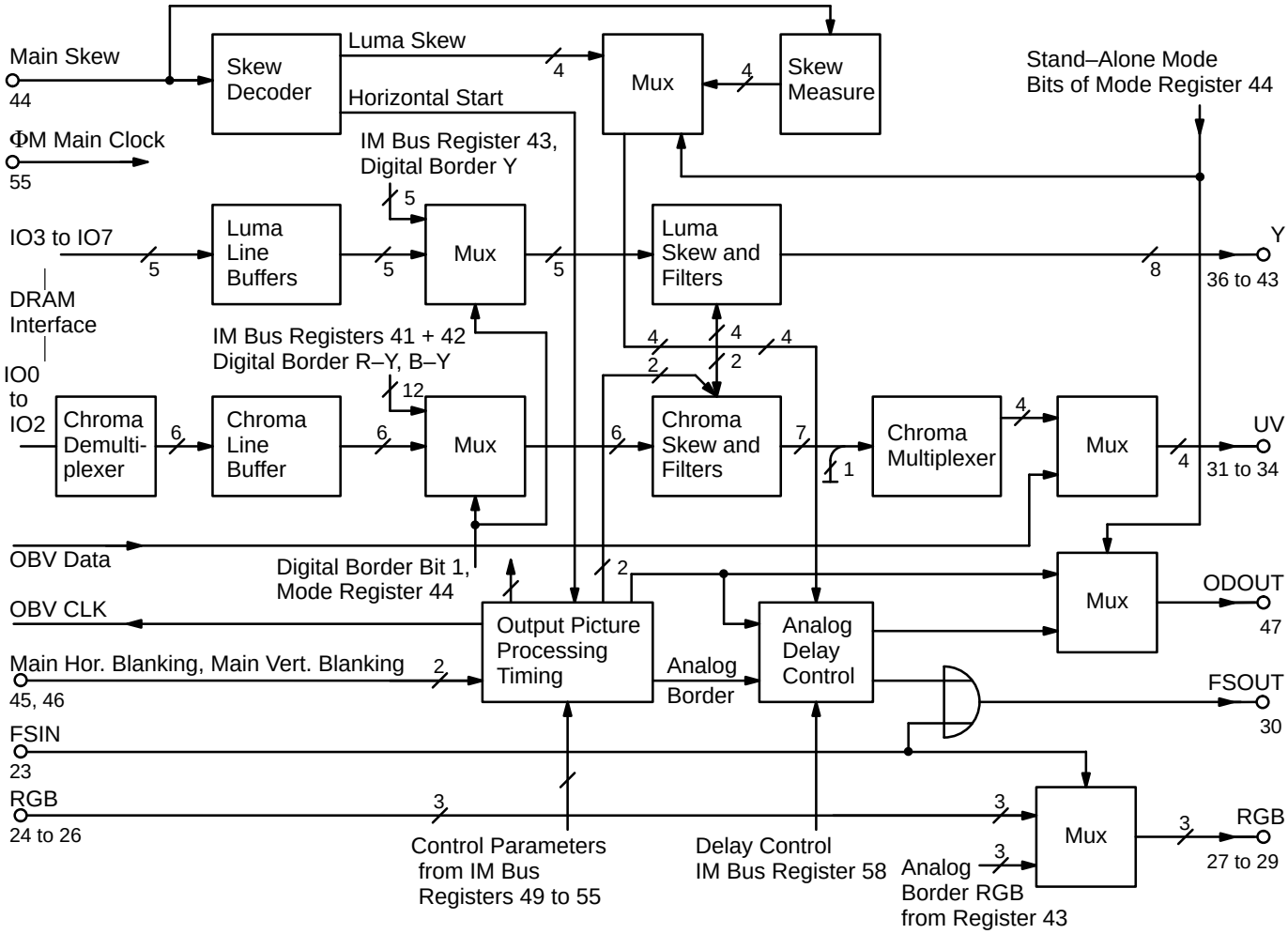

Fig. 3–3: Output picture processing block diagram

3.4.1. PIP 2250 in Various System Applications

3.4.1.1. Digital–Insertion/Stand–Alone Mode

If the main picture is digital, it would share the same output YUV bus with the PIP 2250. The ODOUT outputs disable output of the PIP would then behave like a bus request signal to the VPU that generates the main picture and determines when PIP may have access to the output YUV bus. This mode of operation for merging the small picture with the main picture is defined as “digital insertion” (Fig. 3–4). In this mode, timing signals main skew data, main horizontal blanking and main vertical blanking are generated by the DPU 2553 or DPU 2554 Deflection Processors for the digital main picture.

However, if the main picture is analog, the PIP 2250 would access the output YUV bus alone. The merging of the small picture with the main picture would have to be by analog switching between the RGB of the analog main picture and the RGB output of the VCU for the small picture via the PIP’s ODOUT output. This mode of operation is defined as “stand–alone” (Fig. 3–5).

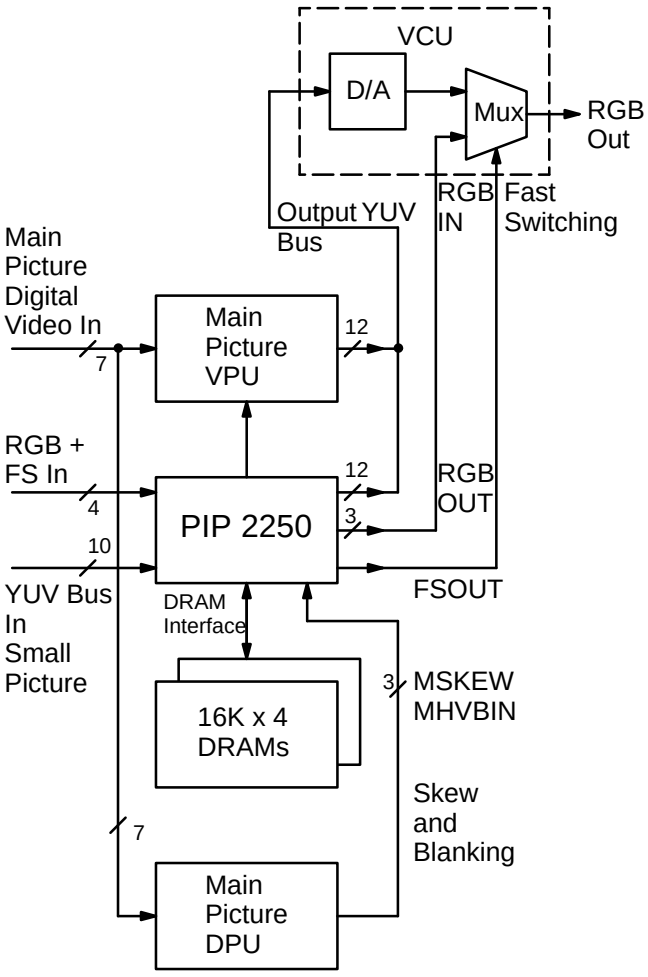

Fig. 3–4: Digital–insertion mode block diagram

In stand–alone mode operation, there is no DPU to generate the main skew data, main horizontal blanking and main vertical blanking timing signals. Instead, two analog signals, main horizontal and main vertical, are available from the analog main picture and share the pins for main horizontal blanking and main vertical blanking, respectively. The main horizontal is a negative–pulsed signal derived from the analog main picture with the main picture horizontal frequency and its trailing edge defines the horizontal start. In this case, luma skew data is generated by the skew measurement block (Fig. 3–3) which measures the phase/time difference between clock trailing edge and the main horizontal trailing edge in resolution of 1/16 of the clock period. Bit 5 of register 44 defines the digital–insertion/stand–alone mode operation.

In digital–insertion mode, the main picture VPU controls the chroma bus timing with PIP and VCU as slave. It also transmits the 72–bit data during vertical blanking.

In stand–alone mode, since PIP is the only master on the output YUV bus, it controls the chroma bus timing and transmits the 72–bit data during vertical blanking.

Table 3–1 summarizes the input/output status for the chroma bus bit 0 (C0 chroma out/Msync in, pin 31) as a function of digital insertion/stand–alone mode and chroma sync scheme selection.

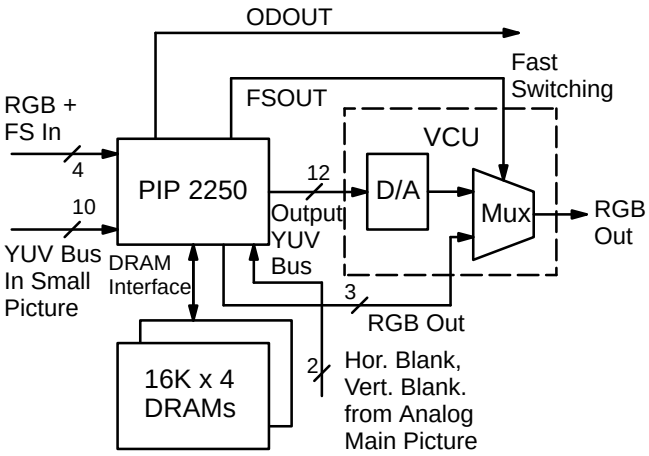

Fig. 3–5: Stand–alone mode block diagram

3.4.1.2. Digital/Analog Border

The border for the small picture may be either digital or analog. The digital border is merged with the small picture inside the PIP with digital correction for skew and output with the small picture at output YUV bus. The analog border is output at the FSOUT Fast Switching Output pin as border timing pulses with time delay based on skew added to the intrinsic delay (Fig. 3–6). Digital border is an inherent part of the small picture while analog border has to be merged with the small picture in the VCU.

Table 3–1: Status of pin 31 depending on operation mode and chroma sync

Mode	Chroma Sync	Pin 31 during horizontal blanking chroma sync window	Pin 31 during vertical blanking chroma sync window
digital insertion	PAL/NTSC	chroma output	sync pulses input
digital insertion	D2–MAC/SECAM	sync pulses input	high–impedance output
stand–alone	PAL/NTSC	chroma output	sync pulses and clocks for 72–bit data output
stand–alone	D2–MAC/SECAM	sync pulses output	clocks for 72–bit data output

Selection of digital/analog border is via bit 1 of register 44. For digital border, LSBs of register 41 to 43 define the luma and chroma values while three MSBs of register 43 define eight different analog borders (see IM bus registers, section 4.2.).

The FSIN Fast Switching Input (pin 23) can be used to switch over the analog RGB outputs (pins 27 to 29) between analog border (supplied by register 43) and external RGB source connected to the analog RGB inputs (pins 24 to 26). If FSIN is High, the analog RGB inputs are connected to the analog RGB outputs. The RGB switch (Fig. 3–6) can also be controlled by software via IM bus register 57 (bit 1, “RGBE”). If RGBE = 1, the external RGB source at pins 24 to 26 is connected to the RGB outputs, pins 27 to 29. If analog border is selected via IM bus register 44 (bit 1, “BDI” = 0), the 3–bit analog RGB border of register 43 is switched to the analog RGB outputs, pins 27 to 29; during the analog border timing is active.

The priority of the external RGB source can be programmed by IM bus register 57 (bit 6, “RGBP”). If RGBP = 1, the priority of the analog RGB inputs and FSIN is higher than the analog border. Figs. 2–22 to 2–25 illustrate the timing waveforms of the ODOUT output and the FSOUT output for different combinations of operating mode and border selection.

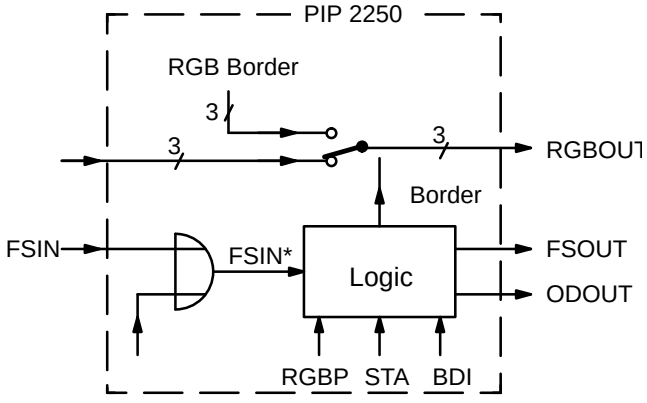

Fig. 3–6: RGB control

To merge analog border with small picture in VCU, the PIP analog RGB outputs are fed to the external RGB inputs of the VCU, and the PIP FSOUT is fed to the VCU Fast Blanking input (Fig. 3–4)

3.4.1.3. Teletext Processing

The PIP 2250 maintains the application of Teletext by TPU Teletext Processors via the PIP external RGB inputs. For this application, the FSIN input should be kept Low.

3.4.1.4. Magnify Mode

The PIP 2250 may display the small picture in a magnify mode wherein a fraction of the small picture is displayed with a magnification factor of 2. Bit 2 of register 44 defines this application.

3.4.1.5. Proscan Processing

The PIP 2250 may also work with the PSP 2210 Progressive–Scan Processor which accepts the YUV bus at normal 4 times color subcarrier rate as input, but outputs pixels at twice the normal rate so that each horizontal line is displayed twice. This is defined as 2H proscan mode and programmable through bit 6 of register 44. In this application, the horizontal deflection rate is doubled by Skew data input containing two horizontal start head codes 001 and 011 in every line. The 001 head code is followed by the primary skew data and 011 by the secondary skew data (Fig. 2–20). The PIP would behave as in a normal digital–insertion application, reacting only to primary skew data so far as skew correction and YUV bus outputs are concerned. However, when analog border is activated, PIP would see doubled deflection rate in the two horizontal starts defined by primary and secondary skew data head codes and generate two sets of analog border pulses at the FSOUT output (Fig. 2–27). In this case, the programming of the border location and horizontal sizes should be half of those in the normal application. In addition, the FSOUT timing for the analog border is delayed by one line to compensate for the vid-

eo signal delay through the PSP 2210 Proscan Processor.

3.4.2. Output Luma Processing

Luma signal processing in output picture processing consists of luma skew interpolation and lowpass filtering. Skew interpolation “un–aligns” the data retrieved from line buffers which had been aligned vertically. The skew interpolation has the following characteristics:

$H(z) = (1 = K1) \cdot z^{-1} + K1 \cdot z^{-2} + K2 \cdot (z^{-1} - 1) \cdot (1 - z^{-2})$

where

K1 = luma skew/16
K2 = C/32
C = 0 for luma skew = 0
C = 1 for luma skew = 1, 2, 14, 15
C = 2 for luma skew = 3, 4, 12, 13
C = 3 for luma skew = 5, 6, 7, 8, 9, 10, 11

Luma lowpass filter has the following response:

$h(z) = 1 + z^{-1}$

Output of luma processing generates 6 bits of data. Two LSBs = 0 are appended to complete the 8–bit luma of output YUV bus.

3.4.3. Output Chroma Processing

Chroma signal processing in output picture processing consists of chroma skew interpolation and lowpass filtering after demultiplexing of 3–bit data from DRAM interface into 6 bits. The skew interpolation has the following characteristics:

$H(z) = (1 - K1) \cdot z^{-2} + K1 \cdot z^{-4} + K2 \cdot (z^{-2} - 1) \cdot (1 - z^{-4})$

where

K1 = chroma skew/16
K2 = C/32
C = 0 for chroma skew = 0
C = 1 for chroma skew = 1, 2, 14, 15
C = 2 for chroma skew = 3, 4, 12, 13
C = 3 for chroma skew = 5, 6, 7, 8, 9, 10, 11

Chroma lowpass filter has the following response:

$h(z) = 1 + z^{-2}$

Again, chroma processing is time–shared by the R–Y and B–Y components at two times the color subcarrier rate. The 7–bit chroma output is then augmented with LSB = 0 and multiplexed into 4–bit at four times the color subcarrier rate for output YUV bus format.

3.4.4. Luma Skew Measurement and Analog Delay Control

As described earlier, data stored in the external DRAMs for each line are aligned vertically with respect to the input picture analog horizontal sync after the input picture processing. In output picture processing, these data have tot be interpolated again for the different skew in the main picture form line to line. However, in stand–alone application ,there is no DPU Deflection Processor in the system to measure the skew data, so the PIP 2250 has to perform the skew measurement between the main picture clock ΦM and the horizontal blanking pulse of the main system, which is applied to pin 45. The skew measurement block measures the phase/time difference between clock trailing edge and the trailing edge of the horizontal blanking pulse at pin 45, in resolution of 1/16 of the ΦM main clock period. This is an analog–to–digital conversion for the skew. Any analog switching control output, like the FSOUT when representing analog border, or ODOUT output in stand–alone mode which is used to switch between analog RGB of main picture and analog RGB small picture, must have its timing modified analogly as a delay be the amount of skew from line to line. This is a digital–to–analog conversion for the skew.

3.4.5. Parameters for Control of Output Picture Processing

Parameters BHS, BLSB and BVS control the location of border while BWI, BFA, BHW,BLSB,BHI and PHI control the sizes of border (Fig. 3–7). For the small picture, parameters PHS1, PHS2, BVS and BHI control the location while PHI and PWI control the picture size.

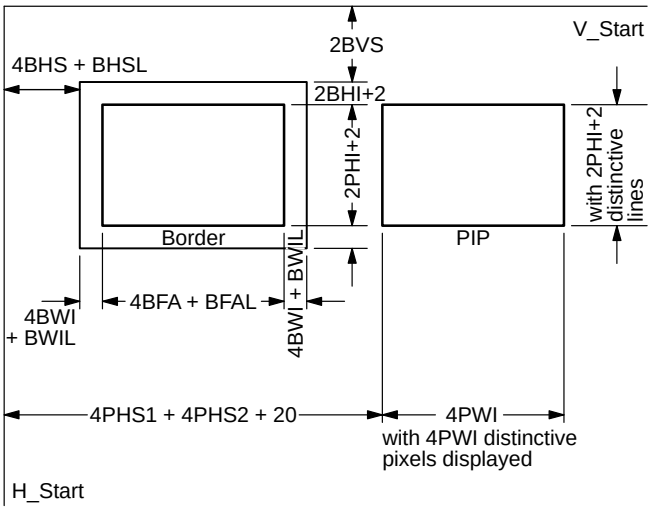

Fig. 3–7: Output picture processing parameters, normal mode. In magnify mode, 2PWI distinctive pixels are displayed horizontally and PHI + 1 lines are displayed vertically.

Notice the border is really comprised of vertical borders and horizontal borders. Therefore parameter BHW is required in addition to BWI and BFA, and BHW + BHWL has to be consistent with 2BWI + BFA + 2BWL + BFAL.

In normal display there are 4PWI distinctive pixels per line and 2PHI + 2 distinctive lines in the small picture. In magnify mode display, there are only 2PWI distinctive pixels per line and PHI + 1 distinctive lines since each pixel is displayed twice, so is each line.

It takes two parameters PHS1 and PHS2 to define the horizontal position of the small picture because of the output line buffer structure (Figs. 3–8 and 3–9). The output line buffer is a fixed–length 224–bit shift register while the number of Bytes transferred per line from external DRAM to this buffer, may be 224 or less. This means data bits near the buffer output end may be garbage and may have to be emptied out. The parameter PHS1 establishes the pixel count from horizontal start to when the line buffer is ready to shift out data. The parameter PHS2 accounts for the number of line buffer shift clocks needed to make the first displayed pixel appear at the line buffer output. This includes emptying out the garbage and even some valid pixels. For example, in magnify mode display, only 2PWI pixels in the line buffer are used for display, and the first pixel to be displayed does not have to be the first valid pixel.

In magnify mode, another parameter RFC is needed. In this mode, each line is displayed twice with the line buffer output fed back to the input as a re–circulating shift register for the second lines. However, the re–circulating clock count has to go by the following equation:

4RFC = 224 – 4PHS2 – 2PWI

in order for data bits to circulate back to the exact same positions as they were in the previous line.

3.5. DRAM Interface

The DRAM interface manages in real-time the tasks of storing (writing) into DRAM the outputs IO0 to IO7 (pins 10 to 17) from input picture processing, retrieving (reading) the reduced picture from DRAM for output picture processing, and refreshing DRAM data. There are two types of read operations – output picture processing read and IM bus read, and two types of write operations – input picture processing write and IM bus write. The priorities of these operations are:

1. output picture processing read
2. input picture processing write
3. IM bus write
4. IM bus read
5. refresh

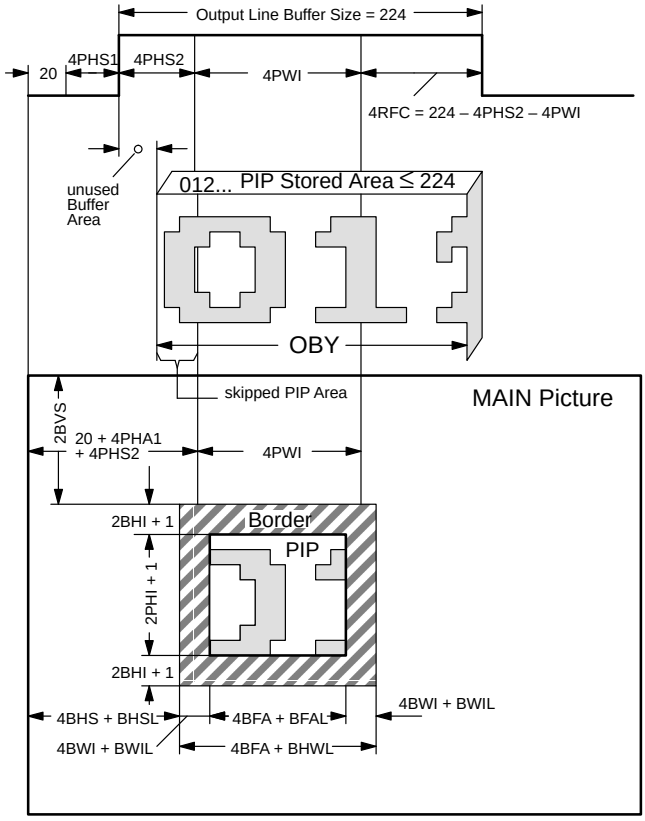

Fig. 3–8: Output picture processing parameters, normal mode

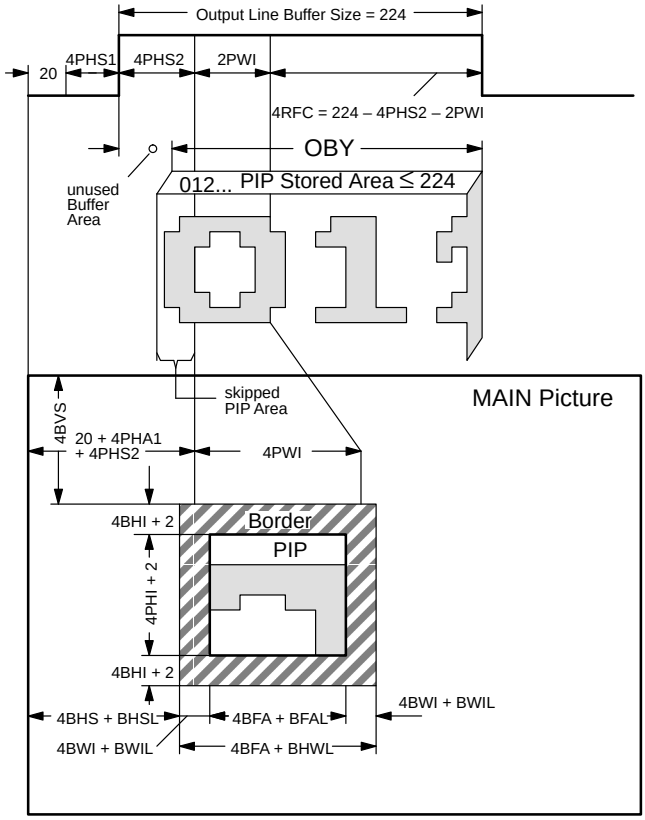

Fig. 3–9: Output picture processing parameters, magnify mode

There are two possibilities of DRAM to be employed, and in both cases page mode must be available:

1. two DRAMs 64 K bit each (16 K x 4) provide the storage capacity for one small picture.

2. two DRAMs 256 K bit each (64 K x 4) provide the storage capacity for up to four small pictures.

Output picture processing read and input picture processing write use page mode to maximize the throughput of DRAM interface. In normal applications, only picture processing read/write and refresh are active. The IM bus read/write are designed in mainly as a system debug tool.

In a page mode read or write, RAS address may be held constant while CAS addresses change for a 32–Byte read or write. Timing diagram (Fig. 2–26) shows the page mode read or write operations. It can be seen that 99 clocks are required for a page mode read or write of 32 Bytes. In between page modes, additional three clocks may be needed if row address is changed. For refresh, five clocks are required for each row.

When 64 K DRAMs are used, bit 0 (MPIP) and bit 4 (IJF) of register 57 should be set to 0. In this case, six of the PIP DRAM CAS address outputs, A1–A6 (LSB to MSB), will be active while CAS A0 and A7 will always be 0. The CAS (A1–A6) together with RAS(A0–A7) will cover the 14–bit address space of the 64 K DRAMs (organized as 16 K x 4).

If 256 K DRAMs are to be used for multiple PIP display, bit 0 (MPIP) of register 57 should be set to 1. Then there may be two different modes of MPIP operations: (A) with bit 4 (IJF) of register 57 set to 0; or (B) with IJF set to 1.

In case (A) of MPIP operation, all eight PIP CAS address outputs are active, with LSB to MSB order of A1–A7, A0. This together with the 8 RAS addresses would cover the 64 K address space of 256 K DRAMs (organized as 64 K x 4). In this mode, up to 4 PIPs may be displayed, each requiring up to 16 K words.

In case (B) of MPIP operation, only 7 PIP CAS address outputs are active, with LSB to MSB order of A1–A7. This together with the 8 RAS addresses would cover one 32 K bank of the total 64 K (two 32 K banks) address space of 256 K DRAMs. However, CAS address output A0 will be equal to the F1 bit in input picture skew data stream for write operation, and be equal to the F1 bit in output picture skew data stream for read operation. Since the F1 bit in skew data identifies the even/odd fields, one of the two 32 K banks in DRAM will be for even field storage/retrieval, and the other for odd field storage/retrieval. In this mode, stored even fields are retrieved for even field display only, and vice versa for the odd fields; thus eliminating the interlace jitter. Up to two PIPs may be displayed each requiring up to 16 K words.

For the reduction mode operation, bit 5 (RED) of register 57 should be set to a 1. In this mode, the input picture vertical reduction rate is increased from 3 to 6 (i.e., every 6 lines, instead of 3, is reduced to one), while the CAS address outputs will be incremented by 2 instead of 1 during read operation (i.e., LSB = CAS A1 will be constant and the next bit = CAS A2 will be incremented). This means the PIP size reduction from 1/9 to 1/36 of regular picture size is achieved vertically in the input picture processing, and horizontally in the output picture processing. It also requires that IPBYTES (input bytes transferred per line) be an even number, and that OPBYTES (output bytes transferred per line) be half of IPBYTES.

3.5.1. Throughput Limitation of DRAM Interface

There is a limit on the values of input Bytes and output Bytes due to DRAM interface throughtput limitation. When displaying the small picture, in the interval of three horizontal lines (3 x 64 μs = 192 μs), 3 x output Bytes must be read and input Bytes must be written. Let

n = input Bytes = output Bytes,

then

$4 (99 n / 32 + 3) \leq 910 \times 3 = 2730,$

where 2730 = worst case number of FP PIP clocks in the three–line interval for NTSC. This results in $n \leq 219$. This is obviously more stringent than the line buffer size limitation of 224.

3.5.2. Access Time Requirements for the DRAMs

For PAL or D2–MAC input pictures, with higher color subcarrier and thus clock frequency used for DRAM interface, throughput is not a problem. But the trade off is the more stringent requirement on DRAM page mode read column access time. From the page mode read timing (Fig. 2–19), it can be seen that

PIP CAS output delay + DRAM page read column access time + PIP data input setup time ≤ 2.0 clocks.

Assuming 20 ns for the sum of PIP CAS output delay and data input setup time, and 50% ± 5% clock duty cycle, an estimate of the DRAM read column access time requirement is

≤ 118 ns for NTSC

≤ 91 ns for PAL

≤ 77 ns for D2–MAC

A commercially available 64 K DRAM like the TMS 4416, with 70 ns column access time, is therefore fast enough for NTSC, PAL and D2–MAC.

4. Control of the PIP 2250 via the IM Bus Interface

4.1. Description of the IM Bus

The INTERMETALL Bus (IM Bus for short) has ben designed to control the DIGIT 2000 ICs by the CCU Central Control Unit. Via this bus the CCU can write data to the ICs or read data from them. This means the CCU acts as a master whereas all controlled ICs are slaves.

The IM Bus consists of three lines for the signals Ident (ID), Clock (CL) and Data (D). The clock frequency range is 50 Hz to 170 kHz. Ident and clock are unidirectional from the CCU to the slave ICs, Data is bidirectional. Bidirectionality is achieved by using open–drain outputs with On–resistances of 150 Ω maximum. the 2.5 kΩ pull–up resistor common to all outputs is incorporated in the CCU.

The timing of a complete IM Bus transaction is shown in Fig. 2–14 and under Recommended Operating Conditions. In the non–operative state, the signals of all three bus lines are High. To start a transaction, the CCU sets the ID signal to Low level, indicating an address transmission, and sets the CL signal to Low level, as well to switch the first bit on the Data line. Thereafter eight address bits are transmitted beginning with the LSB. Data takeover in the slave ICs occurs at the positive edge of the clock signal. At the end of the address Byte the ID signal goes High, initiating the address comparison in the slave circuits. In the addressed slave the IM bus interface switches over to Data read or write, because these functions are correlated to the address.

Also controlled by the address the CCU now transmits eight or sixteen clock pulses, and accordingly one or two Bytes of data are written into the addressed IC or read out from it, beginning with the LSB. The completion of the bus transaction is signalled by a short Low state pulse of the ID signal. This initiates the storing of the transferred data.

It is permissible to interrupt a bus transaction for up to 10 ms.

For future software compatibility, the CCU must write a zero into all bits not used at present. When reading undefined or unused bits, the CCU must adopt “don’t care” behavior.

The PIP 2250’s IM bus interface conforms to the IM bus standard developed for earlier devices like the DPU and VPU with one exception that PIP **does not debounce** the inputs.

4.2. IM Bus Addresses of the PIP 2250 and Associated Functions

The following is da description of the PIP registers programmable via the IM bus. All registers are 8–bit wide unless specified otherwise. All addresses are decimal. To conserve address space of IM bus, the PIP registers are organized in two levels. The thirty–some second–level registers are accessed through the three first–level registers only and thus do not occupy must IM bus register space. The three first–level registers are shown in Table 4–1.

The second–level registers contain parameters for programing the input picture processing, output picture processing, and external DRAM interface. Table 4–2 contains the registers for input picture processing (see Fig. 3–2). The horizontal size for input picture processing is always 224 x 3 pixels. For output picture processing, the registers are contained in Table 4–3 (see Fig. 3–7). The registers for external DRAM interface are shown in Table 4–4, and the mode registers in Tables 4–5 to 4–7.

Table 4–1: First–level registers

Address	Direction	Name	Description
217	Write	PIP_ADDR	second–level register address
218	Read	PIP_R_D	second–level register read data
219	Write	PIP_W_D	second–level register write data

Table 4–2: Input picture processing registers (Direction is always “Write”)

Address	Name	Description
31	IHS	horizontal start position
32	IVS	vertical start position
33	IVSI	vertical size
56	IYD	luma filter delay compensation
59	IBL	input horizontal blanking pulsewidth

Table 4–3: Input picture processing registers (Direction is always “Write”)

Address	Name	Description
40	RFC	number of clocks for 224–Byte buffer refresh, 4RFC = 224 – 4PHS2 – 2PWI
41	BBY	6–bit B–Y for digital border via IM bus D0 to D5
41	OYD	2–bit phase adjust between luma and chroma via IM bus D6 and D7
42	BRY	6–bit R–Y for digital border via IM bus D0 to D5
42	PEA	2–bit for peaking filter in input picture processing via IM bus D6 and D7
43	BOY	5–bit luma for digital border via IM bus D0 to D4
43	RGB	3–bit RGB analog border via IM bus D5 to D7
45	BHS	8 MSBs of border horizontal start position
46	BWI	8 MSBs of vertical border width
47	BFA	8 MSBs of frame width within border
49	BLSB	LSBs for registers BHS, BWI, BFA and BHW, where
	BFAL	bits 2 and 3 are the two LSBs for parameter BFA
	BWIL	bits 4 and 5 are the two LSBs for parameter BWI
	BHSL	bits 6 and 7 are the two LSBs for parameter BHS
50	PHS1	part 1 of picture horizontal start position
51	PHS2	part 2 of picture horizontal start position
52	PWI	picture width
53	BVS	border vertical start position
54	BHI	horizontal border height
55	PHI	frame height within border
58	BRI	brightness control for PIP (bits 0 to 5)
60	OBL	output horizontal blanking pulsewidth

Table 4–4: External DRAM interface registers

Address	Direction	Name	Description
10	Write IBY	IP_BYTES	No. of Bytes for IP transfer/line
11	Write IRA	IP_RAS	IP RAS starting address
12	Write ICA	IP_CAS	IP CAS starting address
13	Write OBY	OP_BYTES	No. of Bytes for OP transfer/line
14	Write ORA	OP_RAS	OP RAS starting address
15	Write OCA	OP_CAS	OP CAS starting address
16	Write IMR	IMB_RAS	IM bus read/write RAS starting address
17	Write IMC	IMB_CAS	IM bus read/write CAS starting address
18	Write IRD	IMB_W_D	IM bus write data
19	Read IWD	IMB_R_D	IM bus read data

Table 4–5: Mode register 1 (Address 44 MODE_REG_1) Description applies if bit = 1

Bit	Name	Description
0	PON	turn on PIP
1	BDI	border digital
2	MON	magnify mode on
3	OPN	output chroma sync: PAL/NTSC
4	IPN	input chroma sync: PAL/NTSC
5	STA	stand–alone operation
6	PSC	2H proscan
7	TEST	test

Table 4–6: Mode register 2 (Address 57 MODE_REG_2) Description applies if bit = 1

Bit	Name	Description
0	MPIP	select 64 K x 4 DRAMs
1	RGBE	enable external RGB
2	DVF	disable vertical filter for input processing
3	POL	port 1 (pin 46)
4	IJF	interlace jitter free mode (full frame store)
5	RED	reduced mode on
6	RFBP	external RGB priority
7	DPK	disable input processing peaking filter

Table 4–7: Mode register 3 (Address 58 MODE_REG_3) Description applies if bit = 1

Bit	Name	Description
6	AFP	alternate field processing
7	EDL	enable delay ODOUT delayed by one clock

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