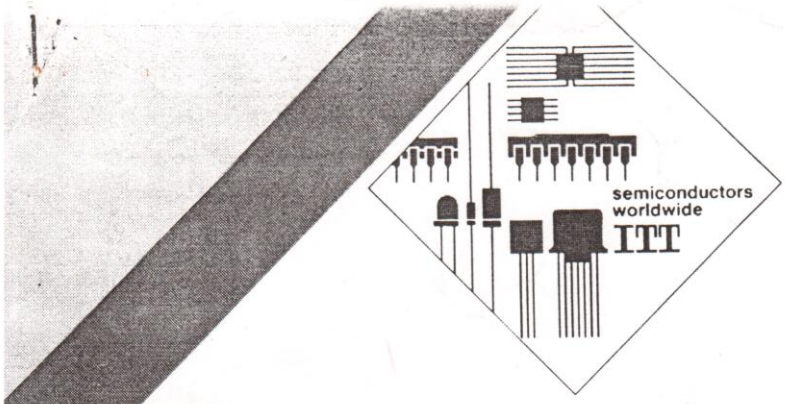

SAJ300R

IC for Quartz-Controlled Clocks with Digital Adjustment

semiconductors ITT

CMOS circuit for RF Quartz Clocks with Digital Adjustment and 0. 5 Hz Output

The monolithic integrated CMOS circuit SAJ300R is intended for use in cristal-controlled clocks operating on 12 V (6 to 16. 5 V) supply voltage.
It comprises an oscillator circuit, a fixed 4:1 frequency divider, a variable 21 stage divider with an adjustment range of 2^{21}:1 to $(2^{21}+2^{9})$:1 and a motor driver stage. An integrated Zener diode with approximately 17 V operating voltage protects the IC against voltage peaks on the supply voltage.
Apart from the crystal the oscillator requires no additional components.
The trimmer capacitor previously needed for frequency adjustment has been omitted and this simplifies the layout of the clock. The function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC and used to set the correct output frequency. For this purpose, seven adjustment terminals are provided on the SAJ300R: they are used to set the divider ratio to the required value with an accuracy of 10^{6}.
With an oscillator frequency of 4. 194812 MHz, the series-connected push-pull output stage supplies a symmetrical square wave signal with a pulse duty factor of 0. 5 and a repetition frequency of 0. 5 Hz if the variable frequency divider is set to the centre.
Due to the differentiating effect of the motor capacitor pulses of alternate direction and one second distance originate in the motor coil.
The adjustable frequency divider has been designed in such a way that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 14. If one ore more adjustment terminals are grounded (taken to pin 13), the output frequency decreases. Pin 7 gives the smallest adjustment of 1. 9 ppm. Pin 6 affords the next-larger step of 3. 8 ppm and so forth, up to pin 1 which enables an adjustment step of 122 ppm to be obtained. Thus, if all adjustment terminals are grounded, the output frequency is reduced by 242 ppm.
The by-four-divided oscillator frequency may be checked at a separate test terminal M (pin 8) non-reactive with respect to the oscillator. Based on this check the output frequency and consequently the accuracy of the clock may be adjusted at the terminals 1 to 7 by means of the variable frequency divider.

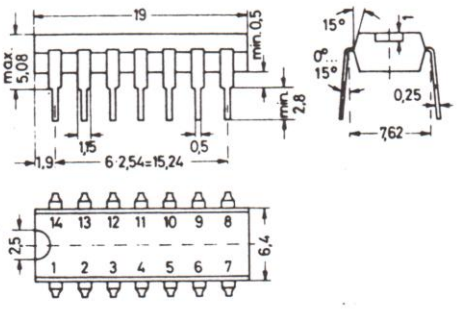

Fig. 1:
SAJ 300 R in dual in-line (Dil) plastic TO-116 package
20 A 14 according to DIN 41 866

Weight approximately 1.1 g
Dimensions in mm

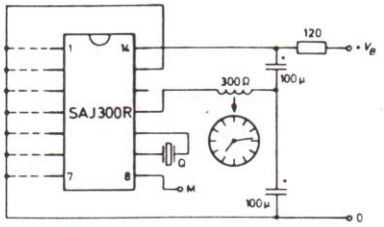

Fig. 2:
Operating circuit of the SAJ300R

Electrical Characteristics

All Voltages referred To pin 13.

Absolute Maximum Ratings

	Symbol	Value	Unit
Supply Voltage	V_B	-0.3 to +18	V
Output Current	I_{11}	60	mA
Current Load of Test Output	I_8	0.1	mA
Power Dissipation at T_A=25 °C	P_{tot}	300	mW
Ambient Operating Temperature Range	T_A	-45 to +85	°C
Storage Temperature Range	T_S	-55 to +125	°C

Recommended Operating Conditions

	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{14}	6	12	16.5	V
Parallel Resonance Frequency of the Quartz at C_L = 16 pF	f_p	-	4.194812	-	MHz
Effective Series Resistance of the Quartz at C_L = 16 pF	R_r	-	-	150	Ω
Output Load Resistance	R_L	250	-	-	Ω

Characteristics at V_{14} = 12 V, Quartz 4.194812 MHz, T_A = 25 °C

	Symbol	Value	Unit
Current Consumption at open Output	I_{14}	3	mA
Output Frequency at Centre Position of the Variable Divider	f_o	0.5	Hz
Frequency at Test Output	f_M	1.048703	MHz
Range of Output Frequency Adjustment	$\Delta f_o/f_o$	±121	ppm
Accuracy of Output Frequency Adjustment	df_o/f_o	±0.95	ppm
Output Pulse Duration	t_o	1	s
Output Resistance at V_{14} = 6 V	r_o	100	Ω