INTEGRATED MOST LEVEL SENSOR

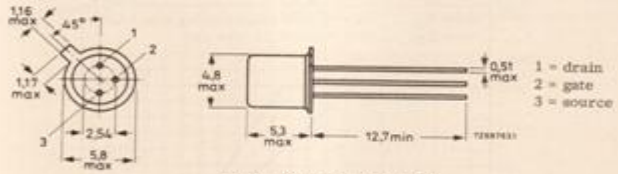
The TAA320A is a silicon monolithic integrated circuit, consisting of a p-channel enhancement type MOS transistor and an n-p-n transistor, in a TO-18 metal envelope. The device is intended for level sensors with a very high input resistance (e.g. timing circuits, thermostats, liquid level sensors, flame control circuits).

QUICK REFERENCE DATA					
Drain-source voltage (V_{GS} = 0)		$-V_{DSS}$	max.	20	V
Drain current		$-I_D$	max.	60	mA
Gate-source voltage [1] $-I_D$ = 10 mA; $-V_{DS}$ = 10 V	group 1:	$-V_{GS}$	typ.	10,6	V
				10,0 to 11,2	V
	group 2:	$-V_{GS}$	typ.	11,3	V
				10,7 to 11,9	V
	group 3:	$-V_{GS}$	typ.	12,0	V
				11,4 to 12,6	V
	group 4:	$-V_{GS}$	typ.	12,7	V
				12,1 to 13,3	V
Gate cut-off current at T_{amb} = 25 °C					
$-V_{GS}$ = 20 V; I_D = 0		$-I_{GSO}$	typ.	1	pA
$-V_{GS}$ = 20 V; V_{DS} = 0		$-I_{GSS}$	typ.	1	pA

PACKAGE OUTLINE

Dimensions in mm

TO-18 (SOT-18/13)

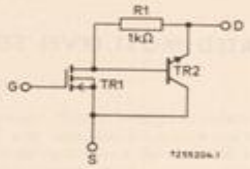


source connected to the case

Accessories supplied on request: 56246; 56263

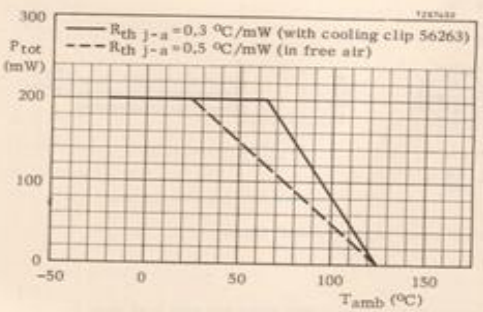
[1] For explanation of the group codefication see note b on page 3.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage (V_{GS} = 0)	$-V_{DSS}$	max.	20	V
Gate-source voltage (I_D = 0)	$-V_{GSO}$	max.	20	V
Non-repetitive peak gate-source voltage (t ≤ 10 ms)	$\pm V_{GSM}$	max.	100	V
Current				
Drain current	$-I_D$	max.	60	mA
Peak drain current (t < 200 ms; δ 0,001)	$-I_{DM}$	max.	100	mA
Temperatures				
Storage temperature	T_{stg}		−65 to +125	°C
Operating ambient temperature (see curve below)	T_{amb}		−20 to +125	°C



CHARACTERISTICS $T_j = 25\ ^{\circ}C$ unless otherwise specified

Drain current					
$-V_{DS} = 20$ V; $V_{GS} = 0$		$-I_{DSS}$	typ.	5	nA
			<	1	μA
Drain-source voltage [1]					
$-I_D = 10$ mA; $-V_{GS} = 20$ V		$-V_{DS}$	<	1	V
$-I_D = 60$ mA; $-V_{GS} = 20$ V		$-V_{DS}$	<	1,5	V
Gate-source voltage (see note b)					
$-I_D = 10$ mA; $-V_{DS} = 10$ V	group 1:	$-V_{GS}$	typ.	10,6	V
			10,0 to 11,2		V
	group 2:	$-V_{GS}$	typ.	11,3	V
			10,7 to 11,9		V
	group 3:	$-V_{GS}$	typ.	12,0	V
			11,4 to 12,6		V
	group 4:	$-V_{GS}$	typ.	12,7	V
			12,1 to 13,3		V
Gate cut-off current					
$-V_{GS} = 20$ V; $I_D = 0$		$-I_{GSO}$	typ.	1	pA [2]
$-V_{GS} = 20$ V; $V_{DS} = 0$		$-I_{GSS}$	typ.	1	pA [2]

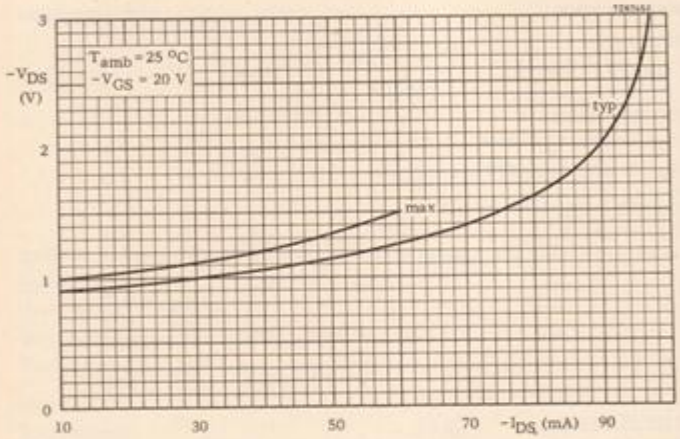
NOTES

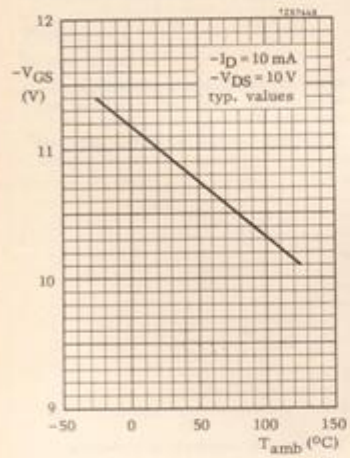
a. The leads are short-circuited by a clip to protect the oxide layer against damage due to accumulation (or build-up) of electrostatic charge on the high resistance gate electrode. The clip should not be removed until after the device is mounted.

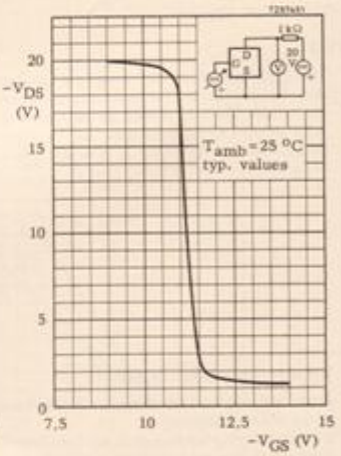
b. As a service to the customer the $-V_{GS}$ group to which a device belongs is identified by a numerical suffix (1, 2, 3 or 4), however, individual groups cannot be ordered separately.

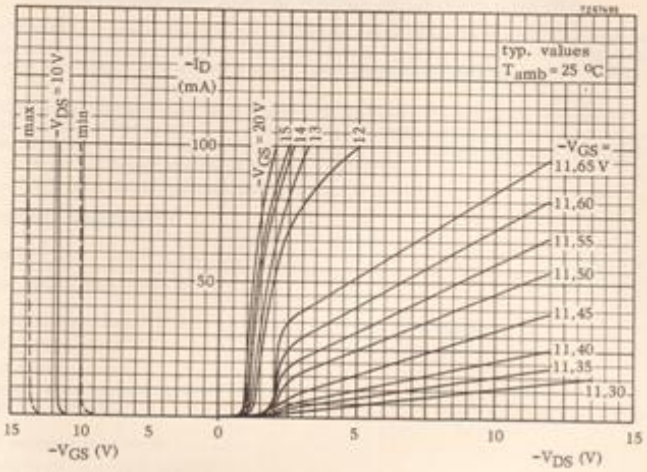
1. See also upper graph on page 4.

2. Being dependent on handling and ambient humidity, the quoted value applies only up to the time of shipping.
Efficient drying treatment is advised before the device is mounted, provided the application requires this low current.








typ. values
T_{amb} = 25 °C
$-I_D$ (mA)
100
50
max
min
$-V_{DS}$ = 10 V
$-V_{GS}$ = 20 V
15
14
13
12
$-V_{GS}$ =
11,65 V
11,60
11,55
11,50
11,45
11,40
11,35
11,30
15
10
5
0
5
10
15
$-V_{GS}$ (V)
$-V_{DS}$ (V)